HITACHI

No. 0108

C28W440N
CL28W440AN
C28WF540N
C32WF540N

SERVICE MANUAL
MANUEL D'ENTRETIEN
WARTUNGSHANDBUCH

CAUTION:

Before servicing this chassis, it is important that the service technician read the "Safety Precautions" and "Product Safety Notices" in this service manual.

ATTENTION:

Avant d'effectuer l'entretien du châassis, le technicien doit lire les «Précautions de sécurité» et les «Notices de sécurité du produit» présentés dans le présent manuel.

VORSICHT:

Vor Öffnen des Gehäuses hat der Service-Ingenieur die „Sicherheitshinweise" und „Hinweise zur Produktsicherheit" in diesem Wartungshandbuch zu lesen.

Data contained within this Service manual is subject to alteration for improvement.

Les données fournies dans le présent manuel d'entretien peuvent faire l'objet de modifications en vue de perfectionner le produit.

Die in diesem Wartungshandbuch enthaltenen Spezifikationen können sich zwecks Verbesserungen ändern.

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

COLOUR TELEVISION
APRIL 2002

DO NOT CHANGE ANY MODULE UNLESS THE SET IS SWITCHED OFF

The mains supply part of the switch mode power supply's transformer is live.
Use an isolating transformer.
The receiver complies with the safety requirements.

SAFETY PRECAUTIONS:

The service of this TV set must be carried out by qualified persons only. Components marked with the warning symbol on the circuit diagram are critical for safety and must only be replaced with an identical component.

- Power resistor and fused resistors must be mounted in an identical manner to the original component.
- When servicing this TV, check that the EHT does not exceed 26kV.

TV set switched off:

Make short-circuit between HV-CRT clip and CRT ground layer.
Short C809 before changing IC800 and IC801 or other components in primary side of the SMPS part.

Measurements:

Voltage readings and oscilloscope traces are measured under the following conditions:
Antenna signal's level is 60dB at the color bar pattern from the TV pattern generator. (100% white, 75% color saturation)
Brightness, contrast, and color are adjusted for normal picture performance.
Mains supply, 220VAC, 50Hz.

PERI-TV SOCKET

SCART 1 PINING

1 Audio right output	0.5Vrms / 1K
2 Audio right input	0.5Vrms / 10K
3 Audio left output	0.5Vrms / 1K
4 Ground AF	
5 Ground Blue	
6 Audio left input	0.5Vrms / 10K
7 Blue input	0.7Vpp / 75ohm
8 AV switching input	0-12VDC /10K
9 Ground Green	
10 -	
11 Green input	0.7Vpp / 75ohm
12 -	
13 Ground Red	
14 Ground Blanking	
15 Red input	0.7Vpp / 75ohm
16 Blanking input	0-0.4VDC, 1-3VDC / 75 Ohm
17 Ground CVBS output	
18 Ground CVBS input	
19 CVBS output	1Vpp / 75ohm
20 CVBS input	1Vpp / 75ohm
21 Ground	

SCART 2 PINING

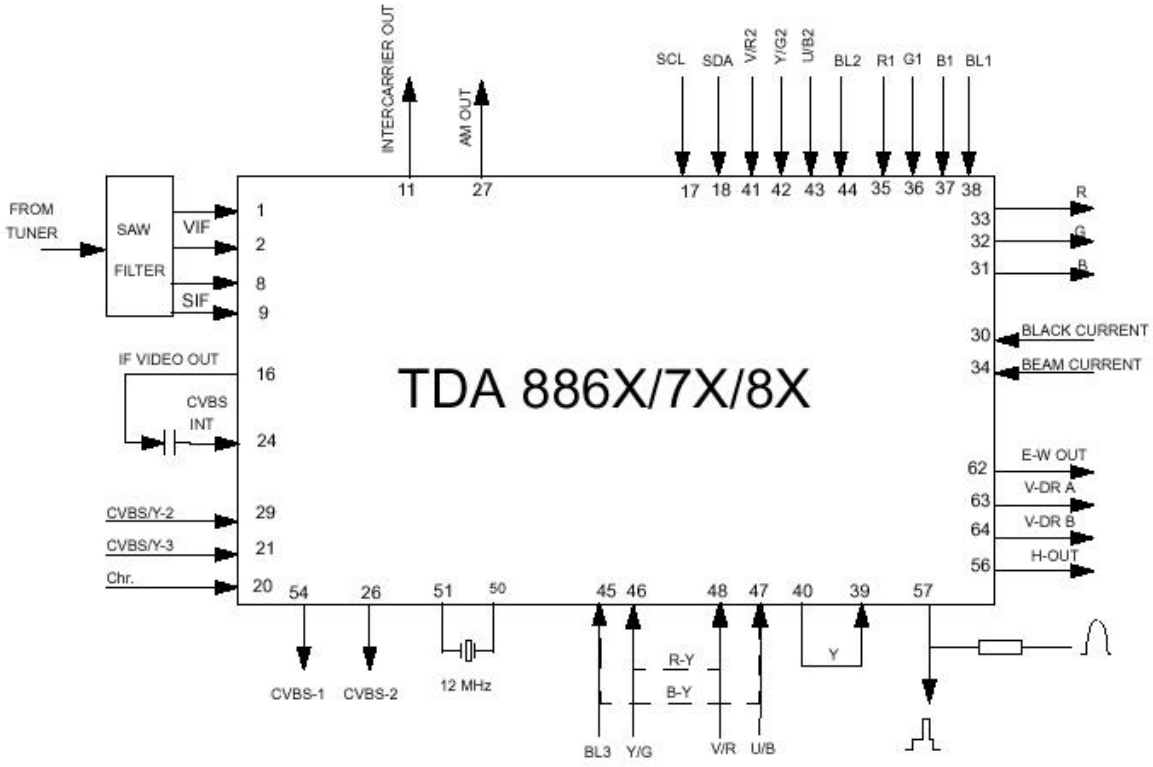
1 Audio right output	0.5Vrms / 1K
2 Audio right input	0.5Vrms / 10K
3 Audio left output	0.5Vrms / 1K
4 Ground AF	
5 Ground Blue	
6 Audio left input	0.5Vrms / 10K
7 -	
8 AV switching input	0-12VDC /10K
9 Ground Green	
10 -	
11 -	
12 -	
13 Ground Red	
14 Ground Blanking	
15 Chroma input (optional)	
16 -	
17 Ground CVBS output	
18 Ground CVBS input	
19 CVBS output	1Vpp / 75ohm
20 CVBS (or Luma) input	1Vpp / 75ohm
21 Ground	

1. INTRODUCTION

This is a 110° chassis capable of driving 28-29",32",33" tubes at appropriate currents. The chassis have, Frequency Controlled Tuning (PLL), and control system for multi-standard (Pal,Secam,BG,DK,L/L',I/I',NTSC,M,N) TV receivers with on-screen-display (OSD) for all relevant control functions. The system is based on the 'one-chip' I²C bus controlled video processing/deflection IC TDA8885 which also controls sound.
German stereo and Nicam is detected and processed by the MSP 3410 G. Dolby sound is processed by MSP 3452 G, virtual dolby by MSP 3411G, BTSC Stereo by MSP 3420G (or MSP 3440G) IC's by option. All sound processors also control the sound volume, balance, tone and spatial stereo effect.
The user-interface is menu based control system with cursor keys. Only for some functions the colour keys are needed: This means that some of the functions can also be operated from the local keyboard (i.e. Vol -, Vol +, P -, P+ and Menu).
Teletext is done by the microcontroller on-chip teletext module.Fastext/Toptext(8page),One page are optional.

2. SMALL SIGNAL PART WITH TDA8885

The TDA8885 combines all small signal functions required for a colour TV receiver.



2.1. *Vision IF amplifier*

The IF-amplifier contains 3 ac-coupled control stages with a total gain control range, which is higher then 66 dB. The sensitivity of the circuit is comparable. The video signal is demodulated by means of an alignment-free PLL carrier regenerator with an internal VCO. This VCO is calibrated by means of a digital control circuit, which uses the clock frequency of the m-Controller/Teletext decoder as a reference. The frequency setting for the various standards (33.4, 33.9, 38, 38.9, 45.75 and 58.75 MHz) is realised via the I²C-bus. To get a good performance for phase modulated carrier signals the control speed of the PLL can be increased by means of the FFI bit. The AFC output is generated by the digital

control circuit of the IF-PLL demodulator and can be read via the I²C bus. For fast search tuning systems the window of the AFC can be increased with a factor 3. The setting is realised with the AFW bit. The AGC-detector operates on top sync and top white-level. The demodulation polarity is switched via the I 2 C-bus. The AGC detector capacitor is integrated. The time-constant can be chosen via the I 2 C-bus. The time-constant of the AGC system during positive modulation is rather long to avoid visible variations of the signal amplitude. To improve the speed of the AGC system a circuit has been included which detects whether the AGC detector is activated every frame period. When during 3 field periods no action is detected the speed of the system is increased. For signals without peak white information the system switches automatically to a gated black level AGC. Because a black level clamp pulse is required for this way of operation the circuit will only switch to black level AGC in the internal mode. The circuit contains a video identification circuit, which is independent of the synchronisation circuit. Therefore search tuning is possible when the display section of the receiver is used as a monitor. However, this Ident circuit cannot be made as sensitive as the slower sync Ident circuit (SL) and we use both Ident outputs to obtain a reliable search system. The Ident output is supplied to the tuning system via the I 2 C-bus. The input of the identification circuit is connected to pin 24, the internal CVBS input. This has the advantage that the Ident circuit can also be made operative when a scrambled signal is received (descrambler connected between the IF video output (pin 16) and pin 24). A second advantage is that the Ident circuit can be used when the IF amplifier is not used The video Ident circuit can also be used to identify the selected CBVS or Y/C signal. The switching between the 2 modes can be realised with the VIM bit. The IC contains a group delay correction circuit, which can be switched between the BG and a flat group delay response characteristic. This has the advantage that in multi-standard receivers no compromise has to be made for the choice of the SAW filter. Also the sound trap is integrated within the IC .The centre frequency of the trap can be switched via the I²C-bus. For mono-FM versions it is possible to obtain a demodulated IF video signal which has not passed the sound trap so that an external stereo decoder can be driven. This function is selected by means of the ICO bit (sub-address 28H). The signal is available on pin 27 (audio output pin when ICO = 0). The S/N ratio of the selected video signal can be read via the bits SN1/SN0 in sub-address 03H.

2.2. Video Switches

The circuit has an input for the internal CVBS signal and 2 inputs for external CVBS or Y signals. The circuit has only 1 chroma input so that it is not possible to apply 2 separate Y/C inputs. The selection of the various sources is made via the I²C-bus.Two independently switchable outputs are available. The CVBS1O output is identical to the selected signal that is supplied to the internal video processing circuit and which is used as source signal for a teletext decoder. Both CVBS outputs have an amplitude of 2.0 VP-P . The CVBS2O output is used for CVBS-video output. If the Y/C-3 signal is selected for one of the outputs the luminance and chrominance signals are added so that a CVBS signal is obtained again.

2.3. Sound Circuit

The sound IF amplifier is similar to the vision IF amplifier and has a gain control range of about 66 dB. The AGC circuit is related to the SIF carrier levels (average level of AM or FM carriers) and ensures a constant signal amplitude of the AM demodulator and the QSS mixer. A multiplier realises the single reference QSS mixer. In this multiplier the SIF signal is converted to the intercarrier frequency by mixing it with the regenerated picture carrier from the VCO. The mixer output signal is supplied to the output via a high-pass filter for attenuation of the residual video signals. With this system a high performance hi-fi stereo sound processing can be achieved. To optimise the performance of the demodulator the offset can be compensated by means of an I²C-bus setting. The AM sound demodulator is realised by a multiplier. The modulated sound IF signal is multiplied in phase with the limited SIF signal. The demodulator output signal is supplied to the output via a low-pass filter for attenuation of the carrier harmonics. Remark that QSS output pin is 11.

2.4. Synchronisation circuit

The sync separator is preceded by a controlled amplifier, which adjusts the sync pulse amplitude to a fixed level. These pulses are fed to the slicing stage, which is operating at 50% of the amplitude. The separated sync pulses are fed to the first phase detector and to the coincidence detector. This coincidence detector is used to detect whether the line oscillator is synchronised with the incoming signal and can also be used for transmitter identification. This circuit can be made less sensitive by means of the STM bit. This mode can be used during search tuning to avoid that the tuning system will

stop at very weak input signals. The first PLL has a very high statically steepness so that the phase of the picture is independent of the line frequency. The horizontal drive signal is generated by an internal VCO, which is running at a frequency of 25 MHz. This oscillator is stabilised to that frequency by using the 12 MHz frequency of the crystal oscillator as a reference. The time-constant of the first loop can be forced by the I²C-bus (fast or slow). If required the IC can select the time-constant depending on the noise content of the incoming video signal. The horizontal output signal is generated by means of a second loop, which compares the phase of the internal oscillator signal with the phase of the incoming flyback pulse. The time-constant of this loop is connected externally and can be used as input for a dynamic horizontal phase correction. To obtain a smooth switch-on and switch-off behaviour of the horizontal output stage the horizontal drive signal is switched-on and off via the soft-start/soft-stop procedure. This function is realised by means of a variation of the TON of the horizontal drive pulse. When the soft-start procedure is completed the horizontal output is gated with the flyback pulse so that the horizontal output transistor cannot be switched-on during the flyback time. An additional function of the IC is the 'low-power start-up' feature. For this function a supply voltage with a value between 3 and 5 V must be available at the start-up pin (required current 5 mA typical). When all sub-address bytes have been sent and the POR and XPR flags have been cleared, the horizontal output can be switched-on via the STB-bit (sub-address 24H). In this condition the horizontal drive signal has the nominal TOFF and the TON grows gradually from zero to the nominal value as indicated in the soft-start behaviour. As soon as the 8 V supply is present the switch-on procedure (e.g. closing of the second loop) is continued. The presence of the 8 V supply voltage is indicated by the SUP bit in the I²C -bus output byte 02. The circuit generates a vertical sync pulse. This pulse can be selected on pin 49 via the bits CMB1 and CMB0. In the 100 Hz input processor versions the vertical sync pulse is available on pin 63 and the horizontal pulse on pin 56. Via the I C-bus adjustments can be made of the horizontal and vertical geometry. The vertical sawtooth generator drives the vertical output drive circuit, which has a differential output current. For the E-W drive a single ended current output is available. A special feature is the zoom function for both the horizontal and vertical deflection and the vertical scroll function. When the horizontal scan is reduced to display 4 : 3 pictures on a 16 : 9 picture tube an accurate video blanking can be switched on to obtain well-defined edges on the screen. Overvoltage conditions (X-ray protection) can be detected via the EHT tracking pin. When an overvoltage condition is detected the horizontal output drive signal will be switched-off via the slow stop procedure but it is also possible that the drive is not switched-off and that just a protection indication is given in the I²C-bus output bytes. The choice is made via the input bit PRD. When PRD = 1 and an overvoltage is detected the drive is switched-off and the STB bit is set to 0. Switching on of the drive is only possible when the XPR flag is cleared. The IC has a second protection input on the j2 filter capacitor pin. When this input is activated the drive signal is switched-off immediately and switched-on again via the slow start procedure. For this reason this protection input can be used as 'flash protection'. The drive pulses for the vertical sawtooth generator is obtained from a vertical countdown circuit. This countdown circuit has various windows depending on the incoming signal (50 Hz or 60 Hz and standard or non-standard). The countdown circuit can be forced in various modes by means of the I²C-bus. During the insertion of RGB signals the maximum vertical frequency is increased to 72 Hz so that the circuit can also synchronise on signals with a higher vertical frequency like VGA. To obtain short switching times of the countdown circuit during a channel change the divider can be forced in the search window by means of the NCIN bit. The vertical deflection can be set in the de-interlace mode via the I²C bus.

2.5. Chroma and Luminance processing

The circuit contains a chroma bandpass and trap circuit. The filters are realised by means of gyrator circuits and they are automatically calibrated by comparing the tuning frequency with the reference frequency of the decoder. The luminance delay line and the delay for the peaking circuit are also realised by means of gyrator circuits. The centre frequency of the chroma bandpass filter is switchable via the I²C-bus so that the performance can be optimised for 'front-end' signals and external CVBS signals. During SECAM reception the centre frequency of the chroma trap is reduced to get a better suppression of the SECAM carrier frequencies.

2.6. Colour Decoder

The colour decoder can decode PAL, NTSC and SECAM signals. The internal clock signals for the various colour standards are generated by means of an internal VCO, which uses the 12 MHz crystal

frequency as a reference. Under bad-signal conditions (e.g. VCR-playback in feature mode), it may occur that the colour killer is activated although the colour PLL is still in lock. When this killing action is not wanted it is possible to overrule the colour killer by forcing the colour decoder to the required standard and to activate the FCO-bit (Forced Colour On) in subaddress 21H. The IC contains an Automatic Colour Limiting (ACL) circuit which is switchable via the I²C-bus and which prevents that oversaturation occurs when signals with a high chroma-to-burst ratio are received. The ACL circuit is designed such that it only reduces the chroma signal and not the burst signal. This has the advantage that the colour sensitivity is not affected by this function. The SECAM decoder contains an auto-calibrating PLL demodulator which has two references, viz: the divided 12 MHz reference frequency of the crystal oscillator which is used to tune the PLL to the desired free-running frequency and the bandgap reference to obtain the correct absolute value of the output signal. The VCO of the PLL is calibrated during each vertical blanking period, when the IC is in search or SECAM mode. The reference frequency of the colour decoder is fed to the Fsc output (pin 49) and is used to tune an external comb filter. The base-band delay line is integrated. The demodulated colour difference signals are internally supplied to the delay line. The colour difference matrix switches automatically between PAL/SECAM and NTSC, however, it is also possible to fix the matrix in the PAL standard.

2.7. PICTURE IMPROVEMENT FEATURES

In the TDA 8885 series various picture improvement features have been integrated. These features are:
-Video dependent coring in the peaking circuit. The coring can be activated only in the low-light parts of the screen. This effectively reduces noise while having maximum peaking in the bright parts of the picture.
-Colour Transient Improvement (CTI). This circuit improves the rise and fall times of the colour difference signals. The function is realised by using delay cells with a length of 300 ns.
-Black-stretch. This circuit corrects the black level for incoming video signals, which have a deviation between the black level and the blanking, level (back porch). The time constant for the black stretcher is realised internally
-Blue-stretch. This circuit is intended to shift colour near 'white' with sufficient contrast values towards more blue to obtain a brighter impression of the picture
-White-stretch. This function adapts the transfer characteristic of the luminance amplifier in a non-linear way dependent on the picture content. The system operates such that maximum stretching is obtained when signals with a low video level are received. For bright pictures the stretching is not active.
-Dynamic skin tone (flesh) control. This function is realised in the YUV domain by detecting the colourss near to the skin tone. The correction angle can be controlled via the I² C-bus.

2.8. RGB output circuit and black-current stabilisation

This IC has a very flexible control circuit for RGB input signals, which has the following features:
· Including 3 RGB input, one is dedicated for OSD signals one for scart1,the other one is for RGB applications.
· The RGB-1 input which is intended for OSD signals and which can be controlled on contrast and brightness. By means of the IE1 bit the insertion blanking can be switched on or off. Via the IN1 bit it can be read whether the insertion pin has a high level or not
· To obtain an accurate biasing of the picture tube the 'Continuous Cathode Calibration' system has been included in this IC. Via the I² C-bus a black level offset can be made with respect to the level which is generated by the black current stabilisation system. In this way different colour temperatures can be obtained for the bright and the dark part of the picture.
The black current stabilisation system checks the output level of the 3 channels and indicates whether the black level of the highest output is in a certain window (WBC-bit) or below or above this window (HBC-bit). This indication can be read from the I² C-bus and can be used for automatic adjustment of the Vg2 voltage during the production of the TV receiver.
The control circuit contains a beam current limiting circuit and a peak white limiting circuit. The peak white level is adjustable via the I² C-bus. To prevent that the peak white limiting circuit reacts on the high frequency content of the video signal a low-pass filter is inserted in front of the peak detector. The circuit also contains a soft-clipper, which prevents that the high frequency peaks in the output signal become too high. The difference between the peak white limiting level and the soft clipping level is adjustable via the I² C-bus in a few steps.

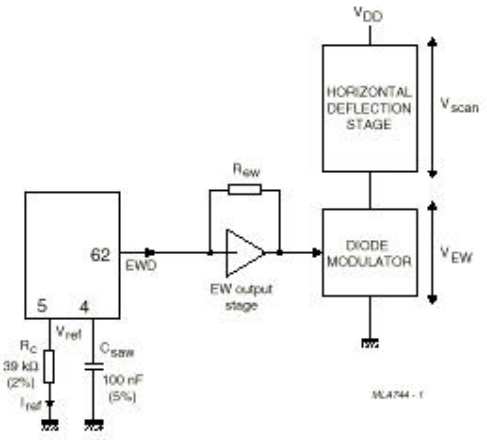
During switch-off of the TV receiver, the black current control circuit generates a fixed beam current. This current ensures that the picture tube capacitance is discharged. During the switch-off period the vertical deflection can be placed in an overseen position so that the discharge is not visible on the screen.

2.9. *EAST – WEST OUTPUT STAGE*

In order to obtain correct tracking of the vertical and horizontal EHT-correction, the EW output stage should be dimensioned as illustrated in Figure. Resistor REW determines the gain of the EW output stage. Resistor Rc determines the reference current for both the vertical sawtooth generator and the geometry processor. The preferred value of Rc is 39 kW which results in a reference current of 100 mA (Vref = 3.9 V).
The value of REW must be:

$R_{EW} = R_C * (V_{scan} / (18* V_{ref}))$

Example: With Vref = 3.9 V; Rc =39 kohm and Vscan = 120 V then REW =68 kohm



2.10 SAW FILTERS

SAW FILTER LIST

SYSTEM&STANDARD	VIDEO (Z 201)	AUDIO (Z 200)
PAL SECAM BG I/I'	K3958M	K9356
PAL SECAM BG DK L/L'	K3953M	K9656M
PAL MN NTSC M	M3953M	M9370

3. TUNER

UV1316 (VHF/UHF) is used as a PLL tuner for only PALM/N. For NTSC M applications UV 1336 are used as the PLL tuner.

Channel coverage of UV1316:

	OFF-AIR CHANNELS		CABLE CHANNELS			
BAND	CHANNELS	FREQUENCY RANGE (MHz)	CHANNELS			FREQUENCY RANGE (MHz)
Low Band	E2 to C	48.25 to 82.25	S01	to	S08	69.25 to 154.25
Mid Band	E5 to E12	175.25 to 224.25	S09	to	S38	161.25 to 439.25
High Band	E21 to E69	471.25 to 855.25	S39	to	S41	447.25 to 463.2

(1). Enough margin is available to tune down to 45.25 MHz.
(2). Enough margin is available to tune up to 863.25 MHz.

Noise	Typical	Max.	**Gain**	Min.	Typical	Max.
Low band	: 5dB	9dB	All channels	: 38dB	44dB	52dB
Mid band	: 5dB	9dB	Gain Taper (of f- air channels)	: -	-	8dB
High band	: 6dB	9dB				

Channel Coverage UV1336:

BAND	CHANNELS	FREQUENCY RANGE (MHz)
Low Band	2 to D	55.25 to 139.25
Mid Band	E to PP	145.25 to 391.25
High Band	QQ to 69	397.25 to 801.25

Noise is typically 6dB for all channels. **Gain** is minimum 38dB and maximum 50dB for all channels.

4. VIDEO SWITCH TEA6415C

In case of three or more external sources are used, the video switch IC TEA6415C is used. The main function of this device is to switch 8 video-input sources on the 6 outputs.
Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of sync. top for CVBS or black level for RGB signals).
Each nominal gain between any input and output is 6.5dB.For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5VDC on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external Resistor Bridge). All the switching possibilities are changed through the BUS.
Driving 75ohm load needs an external resistor.
It is possible to have the same input connected to several outputs.

5. MULTI STANDARD SOUND PROCESSOR

The MSP 34x1G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. signal conforming to the standard by the Broadcast Television Systems Committee (BTSC).
The DBX noise reduction, or alternatively, MICRONAS Noise Reduction (MNR) is performed alignment free.
Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

6. SOUND OUTPUT STAGE WITH TDA 7265

TDA7265 is a class AB dual Audio power amplifier assembled in the multiwatt package.
Mute stand-by function of the audio amplifier can be described as the following; the pin 5 (MUTE/STAND-BY) controls the amplifier status by two different thresholds, referred to +Vs. When Vpin (5) higher than (+Vs - 2.5V) the amplifier is in Stand-by mode and the final stage generators are off. When Vpin (5) is between (+Vs – 2.5V) and (+Vs – 6V) the final stage current generators are switched on and the amplifier is in mute mode. When the Vpin (5) is lower than +Vs – 6V the amplifier is play mode.

7. VERTICAL OUTPUT STAGE WITH STV 9379

The IC TDA9379FA is the vertical deflection booster circuit. Two supply voltages, +14V and –14V are needed to scan the inputs VERT+ and VERT-, respectively. And a third supply voltage, +60V for the flyback limiting are needed. The vertical deflection coil is connected in series between the output and feedback to the input.

8. VIDEO OUTPUT AMPLIFIER TDA6108

The TDA6108Q includes three video output amplifiers is intended to drive the three cathodes of a colour picture tube.

9. COMBFILTER TDA 9181

The TDA 9181 is an adaptive PAL/NTSC comb filter with two internal delay lines, filters, clock control, and input clamps. Video standards PAL B, G, H, I, M and N NTSC M are supported.
Two CVBS input signals can be selected by means of input switch.
In addition to the comb filter the circuit contains an output switch so that a selection can be made between the combed CVBS signal and an external Y/C signal.
The supply voltage is 5V.

10. POWER SUPPLY (SMPS)

The DC voltages required at various parts of the chassis are provided by an SMPS transformer controlled by the IC MC44608, which is designed for driving, controlling and protecting switching transistor of SMPS. The transformer produces 150V for FBT input, +/-14V for audio output IC, S+3.3, S+5V and 8V for TDA8885.

11. POWER FACTOR CORRECTION

The MC33260 is a controller for Power Factor Correction pre-converters meeting international standard requirements in electronic ballast and off–line power conversion applications. Designed to drive a free frequency discontinuous mode, it can also be synchronised and in any case, it features very effective protections that ensure a safe and reliable operation.

12. MICROCONTROLLER SDA555X

12.1. General Features

• Feature selection via special function register
• Simultaneous reception of TTX, VPS, PDC, and WSS (line 23)
• Supply Voltage 2.5 and 3.3 V
• ROM version is used.

12.2. External Crystal and Programmable clock speed

• Single external 6MHz crystal, all necessary clocks are generated internally
• CPU clock speed selectable via special function registers.
• Normal Mode 33.33 MHz CPU clock, Power Save mode 8.33 MHz

12.3. Microcontroller Features

• 8bit 8051 instruction set compatible CPU.
• 33.33-MHz internal clock (max.)
• 0.360 ms (min.) instruction cycle
• Two 16-bit timers
• Watchdog timer
• Capture compare timer for infrared remote control decoding
• Pulse width modulation unit (2 channels 14 bit, 6 channels 8 bit)
• ADC (4 channels, 8 bit)
• UART(rxd,txd)

12.4. Memory

• Up to 128 Kilobyte on Chip Program ROM
• Eight 16-bit data pointer registers (DPTR)
• 256-bytes on-chip Processor Internal RAM (IRAM)
• 128bytes extended stack memory.
• Display RAM and TXT/VPS/PDC/WSS-Acquisition-Buffer directly accessible via MOVX
• UP to 16KByte on Chip Extended RAM (XRAM) consisting of;
- 1 Kilobyte on-chip ACQ-buffer-RAM (access via MOVX)
- 1 Kilobyte on-chip extended-RAM (XRAM, access via MOVX) for user software
- 3 Kilobyte Display Memory

12.5. Display Features

• ROM Character set supports all East and West European Languages in single device
• Mosaic Graphic Character Set
• Parallel Display Attributes
• Single/Double Width/Height of Characters
• Variable Flash Rate
• Programmable Screen Size (25 Rows x 33...64 Columns)
• Flexible Character Matrixes (HxV) 12 x 9...16
• Up to 256 Dynamical Redefinable Characters in standard mode; 1024 Dynamical Redefinable Characters in Enhanced Mode
• CLUT with up to 4096 colour combinations
• Up to 16 Colours per DRCS Character
• One out of Eight Colours for Foreground and Background Colours for 1-bit DRCS and

12.6. ROM Characters

• Shadowing
• Contrast Reduction
• Pixel by Pixel Shiftable Cursor With up to 4 Different Colours
• Support of Progressive Scan and 100 Hz.
• 3 X 4Bits RGB-DACs On-Chip
• Free Programmable Pixel Clock from 10 MHz to 32MHz
• Pixel Clock Independent from CPU Clock
• Multinorm H/V-Display Synchronisation in Master or Slave Mode

12.7. Acquisition Features

• Multistandard Digital Data Slicer
• Parallel Multi-norm Slicing (TTX, VPS, WSS, CC, G+)
• Four Different Framing Codes Available
• Data Caption only limited by available Memory
• Programmable VBI-buffer
• Full Channel Data Slicing Supported
• Fully Digital Signal Processing
• Noise Measurement and Controlled Noise Compensation
• Attenuation Measurement and Compensation
• Group Delay Measurement and Compensation
• Exact Decoding of Echo Disturbed Signals

12.8. Ports

• One 8-bit I/O-port with open drain output and optional I 2 C Bus emulation support (Port0)
• Two 8-bit multifunction I/O-ports (Port1, Port3)
• One 4-bit port working as digital or analogue inputs for the ADC (Port2)
• One 2-bit I/O port with secondary functions (P4.2, 4.3, 4.7)
• One 4-bit I/O-port with secondary function (P4.0, 4.1, 4.4) (Not available in P-SDIP 52)

13. SERIAL ACCESS CMOS 8K (1024*8) EEPROM ST24C08

The ST24C08 is a 8Kbit electrically erasable programmable memory (EEPROM), organised as 4 blocks of 256*8 bits.

The memory is compatible with the I²C standard, two wire serial interface, which uses a bi-directional data bus and serial clock.

The memory carries a built-in 4 bit, unique device identification code (1010) corresponding to the I²C bus definition.

This is used together with 1 chip enable input (E) so that up to 2*8K devices may be attached to the I²C bus and selected individually.

14. CLASS AB STEREO HEADPHONE DRIVER TDA1308

The TDA1308 is an integrated class AB stereo headphone driver contained in a DIP8 plastic package.

The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

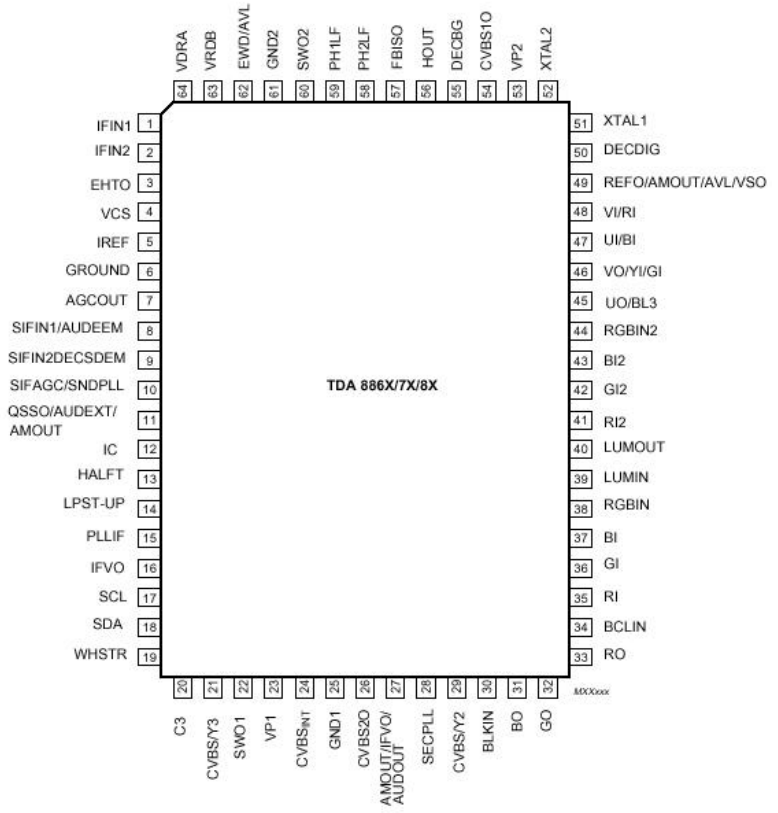
15. SAW FILTERS

Saw filter type	**:**	**Model:**
K9356M	**:**	PAL-SECAM B/G/D/K/I STEREO (AUDIO IF)
K9656M	**:**	PAL-SECAM B/G/D/K/I/L/L' STEREO (AUDIO IF)
K3958M	**:**	PAL-SECAM B/G/D/K/I/L/L' STEREO (VIDEO IF)

16. IC DESCRIPTIONS AND INTERNAL BLOCK DIAGRAM

- TDA8885
- TUNER (UV1315, UV1316)
- TEA6415C
- TDA 7265
- TDA6108Q
- 74HCT32
- MC44608
- SDA5555
- TDA9181
- TCD1102
- ST24C08
- TDA1308
- PCF8583
- MC33260
- STV9379
- MSP34XXG
- LM358N

16.1. TDA8885:



16.1.1. GENERAL DESCRIPTION

The TDA 8885 is I² C-bus controlled singlechip TV processor, which is intended to be applied in PAL/NTSC and multi-standard television receivers. IC contains integrated sound band-pass trap circuits, a switchable group delay correction circuit and a multi-standard colour decoder which needs only one (12 MHz) reference crystal for all standards.
Furthermore various picture improvement features have been included.

16.1.2. FEATURES

Multi-standard vision IF circuit with an alignment-free PLL demodulator without external components
Internal (switchable) time-constant for the IF-AGC circuit
Switchable sound trap and group delay correction circuit for the demodulated CVBS signal
Flexible source selection with CVBS switch and a Y (CVBS)/C input so that a comb filter can be applied
Integrated chrominance trap circuit
Integrated luminance delay line with adjustable delay time
Integrated chroma band-pass filter with switchable centre frequency
Colour decoder which needs only one 12 MHz reference crystal (or external clock signal) for all standards
Blanking of the 'helper signals' for PAL PLUS and EDTV-2
Several picture improvement features.
Internal base-band delay line
Linear RGB input and fast blanking
RGB control circuit with 'Continuous Cathode Calibration', white point and black level offset adjustment so that the colour temperature of the dark and the light parts of the screen can be chosen independently.
Adjustable peak white limiting circuit
Possibility to insert a 'blue back' option when no video signal is available
Horizontal synchronisation with two control loops and alignment-free horizontal oscillator
Vertical count-down circuit
Vertical driver optimised for DC-coupled vertical output stages for improved geometry
Vertical geometry processing.
Low-power start-up for the horizontal drive circuit
I²C-bus control of various functions
QSS sound IF amplifier
- AM sound demodulator
- PAL decoder
- SECAM decoder
- NTSC decoder
- Additional RGB input
- Black stretch and Blue stretch
- Dynamic skin tone control and coring on complete video signal
- Video dependent coring and Colour Transient Improvement
- White stretch and green enhancement
- Horizontal geometry (EW)
- Horizontal and vertical zoom
- Horizontal parallelogram and angle correction
- 2nd CVBS output
- Additional YUV/ RGB input with saturation control
- 2 (I²C- bus controlled) switch outputs, which can be used to switch external circuits

16.1.3. Pin Description

1	IF input 1
2	IF input 2
3	overvoltage protection input
4	vertical sawtooth capacitor
5	reference current input
6	ground
7	tuner AGC output
8	SIF input 1
9	SIF input 2
10	narrow-band PLL filter AGC sound IF
11	QSS out
12	internally connected
13	half tone (contrast reduction)
14	low-power start-up
15	IF-PLL loop filter
16	IF video output
17	serial clock input
18	serial data input/output
19	white stretch capacitor
20	chrominance input (S-VHS)
21	external CVBS/Y 3 input
22	output switch 1 (I²C)
23	main supply voltage (+8V)
24	internal CVBS input
25	ground 1 (colour decoder and synchronisation)
26	CVBS-2 output
27	audio out (volume controlled) / IF video out (3) AM audio output (volume controlled)
28	SECAM PLL decoupling
29	CVBS/Y2 input
30	black-current input
31	blue output
32	green output
33	red output
34	beam current limiter input/V-guard input
35	red input for insertion
36	green input for insertion
37	blue input for insertion
38	RGB insertion input
39	luminance input
40	luminance output
41	2nd R input
42	2nd G input
43	2nd B input
44	2nd RGB insertion input
45	Additional RGB insertion input
46	Additional G input
47	Additional B signal input
48	Additional R signal input
49	Ref. signal out for comb filter applications.
50	decoupling digital supply
51	12 MHz crystal connection
52	12 MHz crystal connection
53	2nd supply voltage (+8 V) (colour decoder, control, synchronisation and geometry)
54	CVBS-1 output
55	bandgap decoupling
56	horizontal output
57	flyback input / sandcastle output
58	phase-2 filter
59	phase-1 filter
60	output switch 2 (I²C)
61	ground 2 (filters, CTI, control and geometry)
62	east-west drive output
63	vertical drive B output
64	vertical drive A output

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltage		8.0		V
I_P	supply current		tbf		mA
Input voltages					
$V_{i(VIF)(rms)}$	video IF amplifier sensitivity (RMS value)		35		V
$V_{i(SIF)(rms)}$	sound IF amplifier sensitivity (RMS value)		60		V
$V_{i(CVBS/Y)(p-p)}$	external CVBS/Y input (peak-to-peak value)		1.0		V
$V_{i(CHROMA)(p-p)}$	external chroma input voltage (burst amplitude)(peak-to-peak value)		0.3		V
$V_{i(RGB)(p-p)}$	RGB inputs (peak-to-peak value)		0.7		V
$V_{i(YI)(p-p)}$	luminance input signal (peak-to-peak value)		1.4/1.0		V
$V_{i(UI)(p-p)}$	U input signal (peak-to-peak value)		1.33/+0.7		V
$V_{i(VI)(p-p)}$	V input signal (peak-to-peak value)		1.05/+0.7		V
Output signals					
$V_{o(IFVO)(p-p)}$	demodulated CVBS output (peak-to-peak value)		2.5		V
$I_{o(AGCOUT)}$	tuner AGC output current range	0		5	mA
$V_{o(QSSO)(rms)}$	sound IF intercarrier output (RMS value)		100		mV
$V_{o(AMOUT)(rms)}$	demodulated AM sound output (RMS value)		500		mV
$V_{o(CVBSO)(p-p)}$	CVBS output voltage video switch (peak-to-peak value)		2.0		V
$V_{o(VO/I)(p-p)}$	? V output/input voltage (peak-to-peak value)		1.05		V
$V_{o(UO/I)(p-p)}$	? U output/input voltage (peak-to-peak value)		1.33		V
$V_{o(YO/I)(p-p)}$	Y output/input voltage (peak-to-peak value)		1.4		V
$V_{o(RGB)(p-p)}$	RGB output signal amplitudes (peak-to-peak value)		2.0		V
$I_{o(HOUT)}$	horizontal output current	10			mA
$I_{o(VERT)}$	vertical output current (peak-to-peak value)		1		mA
$I_{o(EWD)}$	EW drive output current	1.2			mA

16.2. UV1315, UV1316

16.2.1. General description of UV1315:

The UV1315 tuner belongs to the UV 1300 familiy of tuners, which are designed to meet a wide range of applications.
It is a combined VHF, UHF tuner suitable for CCIR systems B/G, H, L, L', I and I'. The low IF output impedance has been designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

16.2.2. Features of UV1315:

Member of the UV1300 family small sized UHF/VHF tuners
Systems CCIR:B/G, H, L, L', I and I'; OIRT:D/K
Voltage synthesised tuning (VST)
Off-air channels, S-cable channels and Hyperband
Standardised mechanical dimensions and pinning
Compact size

PINNING		PIN VALUE
1. Gain control voltage (AGC)	:	4.0V, Max:4.5V
2. Tuning voltage		
3. High band switch	:	5V, Min:4.75V, Max:5.5V
4. Mid band switch	:	5V, Min:4.75V, Max:5.5V
5. Low band switch	:	5V, Min:4.75V, Max:5.5V
6. Supply voltage	:	5V, Min:4.75V, Max:5.5V
7. Not connected		
8. Not connected		
9. Not connected		
10. Symmetrical IF output 1		
11. Symmetrical IF output 2		

Bandswitching table:

	Pin 3	Pin 4	Pin 5
Low band	0V	0V	+5V
Mid band	0V	+5V	0V
High band	+5V	0V	0V

16.2.3. General Description of UV1316:

The UV1316 tuner belongs to the UV 1300 family of tuners, which are designed to meet a wide range of applications.
It is a combined VHF, UHF tuner suitable for CCIR systems B/G, H, L, L', I and I'. The low IF output impedance has been designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

16.2.4. Features of UV1316:

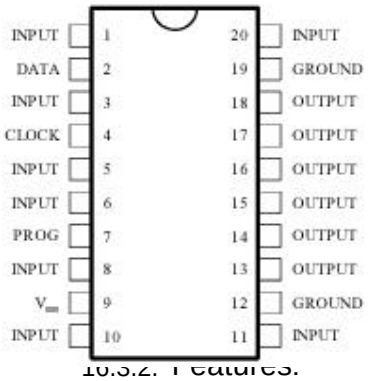
Member of the UV1300 family small sized UHF/VHF tuners
Systems CCIR: B/G, H, L, L', I and I'; OIRT: D/K
Digitally controlled (PLL) tuning via I2C-bus
Off-air channels, S-cable channels and Hyperband
World standardised mechanical dimensions and world standard pinning
Compact size
Complies to "CENELEC EN55020" and "EN55013"

PINNING	**PIN VALUE**
1. Gain control voltage (AGC)	: 4.0V, Max:4.5V
2. Tuning voltage	
3. I²C-bus address select	: Max:5.5V
4. I²C-bus serial clock	: Min:-0.3V, Max:5.5V
5. I²C-bus serial data	: Min:-0.3V, Max:5.5V
6. Not connected	
7. PLL supply voltage	: 5.0V, Min:4.75V, Max:5.5V
8. ADC input	
9. Tuner supply voltage	: 33V, Min:30V, Max:35V
10. Symmetrical IF output 1	
11. Symmetrical IF output 2	

16.3. TEA6415C:

16.3.1. General Description:

The main function of the TEA6415C is to switch 8 video input sources on the 6 outputs.
Each output can be switched to only one of the inputs whereas but any same input may be connected to several outputs.
All switching possibilities are controlled through the I2C-bus.



16.3.2. Features:

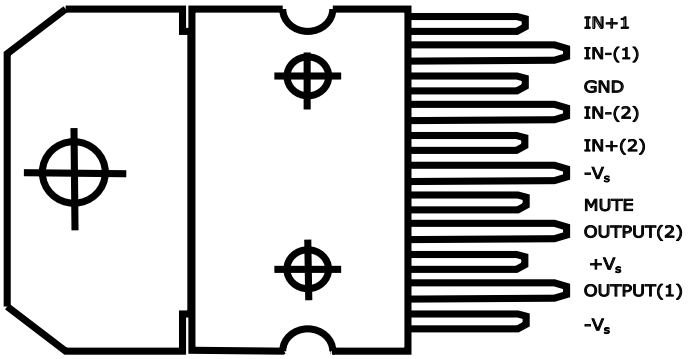
20 MHz Bandwidth

- Cascadable with another TEA6415C (Internal address can be changed by pin 7 voltage)
- 8 inputs (CVBS, RGB, Mac, CHROMA, …)
- 6 Outputs
- Possibility of MAC or chroma signal for each input by switching off the clamp with an external resistor bridge
- Bus controlled
- 6.5dB gain between any input and output
- -55dB crosstalk at 5MHz
- Fully ESD protected

PINNING	PIN VALUE				
1. Input	: Max	: 2Vpp, Input Current	: 1mA,	Max	: 3mA
2. Data	: Low level	: -0.3V Max:1.5V, High level	: 3.0V	Max	: Vcc+0.5V
3. Input	: Max	: 2Vpp, Input Current	: 1mA,	Max	: 3mA
4. Clock	: Low level	: -0.3V Max:1.5V, High level	: 3.0V	Max	: Vcc+0.5V
5. Input	: Max	: 2Vpp, Input Current	: 1mA,	Max	: 3mA
6. Input	: Max	: 2Vpp, Input Current	: 1mA,	Max	: 3mA
7. Prog					
8. Input	: Max	: 2Vpp, Input Current	: 1mA,	Max	: 3mA
9. Vcc	: 12V				
10. Input	: Max	: 2Vpp, Input Current	: 1mA,	Max	: 3mA
11. Input	: Max	: 2Vpp, Input Current	: 1mA,	Max	: 3mA
12. Ground					
13. Output	: 5.5Vpp,	Min : 4.5Vpp			
14. Output	: 5.5Vpp,	Min : 4.5Vpp			
15. Output	: 5.5Vpp,	Min : 4.5Vpp			
16. Output	: 5.5Vpp,	Min : 4.5Vpp			
17. Output	: 5.5Vpp,	Min : 4.5Vpp			
18. Output	: 5.5Vpp,	Min : 4.5Vpp			
19. Ground					
20. Input	: Max : 2Vpp, Input Current		: 1mA,	Max	: 3mA

16.4. TDA7265:

The TDA7265 is a 25W+25W stereo sound amplifier with mute/stand-by facility. STPA control signal coming from microcontroller (when it is at high level) activates the mute function. IC is muted when mute port is at low level. Two stereo audio signals coming from audio module is injected to the inputs of the IC and a power of 12Wrms (10%) is obtained. An external pop-noise circuitry pulls AF inputs of the IC in order to eliminate pop noise when TV is turned on or off via mains supply connection. It is possible to adjust the gain of the amplifiers by feedback external resistors.



16.4.1 Features

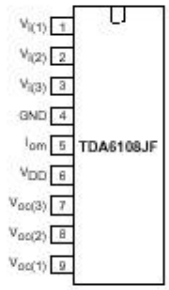
Wide supply voltage range (up to 50V ABS Max.)
Split supply
High output power: 25+25 W @ TDA = 10%, R_L = 8ohm, V_S = ±20V
No pop at turn-on / off
Mute (pop free)
Stand-By feature (low I_Q)
Few external components
Thermal overload protection
Adjustable gain via an external resistor

16.4.2. Pinning:

1. Output (1)
2. +Vs
3. Output (2)
4. Mute / St-By
5. -Vs
6. Input (2)
7. Ground
8. Input (1)

16.5. TDA6108Q:

The TDA6108Q consists of three monolithic video output amplifiers. The amplifier can be seen as an operational amplifier with negative feedback. The advantage of negative feedback is that the amplifier characteristics do not play an important role up to certain frequencies. The internal flash diodes protect the amplifiers against flash over in the picture tube. The only protections required at the cathode outputs are a flash resistor and a spark gap. Furthermore, the device needs only one power supply voltage (Vdd). The TDA6108Q is provided with a black current data pin.



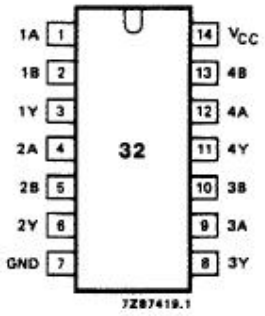
16.5.1. Features:

No external components, only the well known supply decoupling
Very simple application with a variety of colour decoders
Black-current measurement output for automatic black current stabilisation
Only one supply voltage needed
Internal protection against positive appearing CRT flash-over discharges
Protection against ESD
Internal reference voltage
Thermal protection
Controllable switch-off behaviour

PINNING	**PIN VALUE**
1. Inverting input 1	:2Vpp
2. Inverting input 2	:2Vpp
3. Inverting input 3	:2Vpp
4. Ground	
5. BSC-output	:Max:7V
6. Supply voltage	:200VDC
7. Cathode output 3	:20mA, 100Vpp
8. Cathode output 2	:20mA, 100Vpp
9. Cathode output 1	:20mA, 100Vpp

16.6. 74HCT32 (For audio switching in multiple audio input models)

The 74HC/HCT32 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC. The 74HC/HCT32 provide the 2-input OR function.Used for audio switching purposes.



16.6.1. Pinning

1, 4, 9, 12 : 1A to 4A data inputs
2, 5, 10, 13 : 1B to 4B data inputs
3, 6, 8, 11 : 1Y to 4Y data outputs
7 : GND ground (0 V)
14 : V_{CC} positive supply voltage

For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} ? ? 1.5 V

16.7. MC44608

16.7.1. General Description:

The MC44608 is a high performance voltage mode controller designed for off–line converters. This high voltage circuit that integrates the start–up current source and the oscillator capacitor, requires few external components while offering a high flexibility and reliability.
The device also features a very high efficiency stand–by management consisting of an effective Pulsed Mode operation. This technique enables the reduction of the stand–by power consumption to approximately 1W while delivering 300mW in a 150W SMPS.

- Integrated start–up current source
- Lossless off–line start–up
- Direct off–line operation
- Fast start–up

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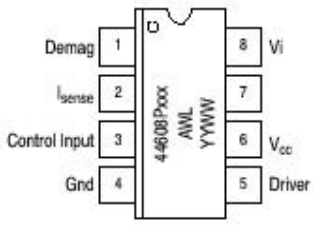
- Integrated start–up current source
- Lossless off–line start–up
- Direct off–line operation
- Fast start–up



16.7.2. General Features

- Flexibility
- Duty cycle control
- On chip oscillator switching frequency 40, or 75kHz
- Secondary control with few external components

Protections

- Maximum duty cycle limitation
- Cycle by cycle current limitation
- Demagnetisation (Zero current detection) protection
- "Over V CC protection" against open loop
- Programmable low inertia over voltage protection against open loop
- Internal thermal protection

GreenLine Controller

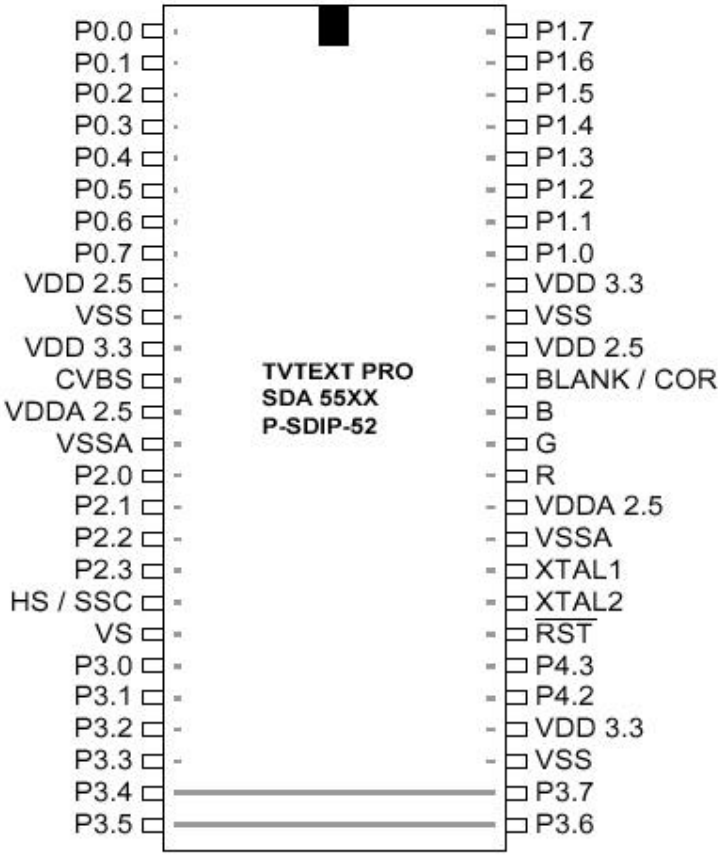
- Pulsed mode techniques for a very high efficiency low power mode
- Lossless start-up
- Low dV/dT for low EMI radiation's

PINNING	**PIN VALUE**
1. Demagnetisation	Zero cross detection voltage: 50 mV typ.
2. I Sense	Over current protection voltage 1V typ.
3. Control Input	Min: 7.5V Max.: 18V
4. Ground	Iout $2A_{p-p}$ during scan $1.2A_{p-p}$ during flyback
5. Driver	Output resistor 8.5 Ohm sink 15 Ohm source typ.
6. Supply voltage	Max:16V (Operating range 6.6V-13V)
7. No connection	
8. Line Voltage	Min:50V Max:500V

16.8. SDA5555: (controller)

16.8.1. General Description:

- Feature selection via special function register
- Simultaneous reception of TTX, VPS, PDC, and WSS (line 23)
- Supply Voltage 2.5 and 3.3 V

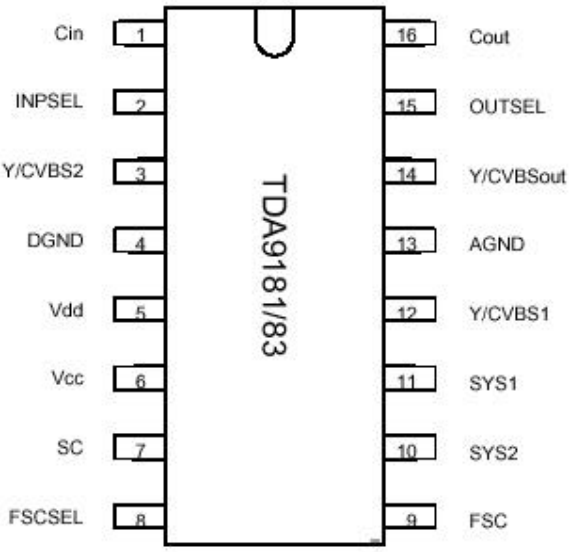


PINNING

1	Comb Filter Standard Selection 1	Low Level :	0V	High Level : 3.3 V
2	Key 2	Low Level :	0V	High Level : 3.3 V
3	Key 1	Low Level :	0V	High Level : 3.3 V
4	Loc.key.switch input	Low Level :	0V	High Level : 3.3 V
5	Loc.key.switch input	Low Level :	0V	High Level : 3.3 V
6	Loc.key.switch input	Low Level :	0V	High Level : 3.3 V
7	Loc.key.switch input	Low Level :	0V	High Level : 3.3 V
8	Mute output	Low Level :	0V	High Level : 3.3 V
9	Digital supply voltage	2.5 V		
10	Ground			
11	Digital supply voltage	3.3 V		
12	CVBS input	1 Vpp		
13	Analogue supply voltage	2.5 V		
14	Analogue ground			
15	Wake Interrupt	Low Level :	0V	High Level : 3.3 V
16	AV-1 status input	Low Level :	0V	High Level : 3.3 V
17	AV-2 status input	Low Level :	0V	High Level : 3.3 V
18	Shortcut protection	Low Level :	0V	High Level : 3.3 V
19	SAND input	Low Level :	0V	High Level : 3.3 V
20	ODD/EVEN output	Low Level :	0V	High Level : 3.3 V
21	DVD 12 V Sense	Low Level :	0V	High Level : 3.3 V
22	Not used			
23	Idle Off	Low Level :	0V	High Level : 3.3 V

24	IR-input	Low Level : 0V	High Level : 3.3 V
25	Data output	Low Level : 0V	High Level : 3.3 V
26	Clock signal output	Low Level : 0V	High Level : 3.3 V
27	Stand-By Mode selection	Low Level : 0V	High Level : 3.3 V
28	Not used		
29	Ground		
30	Digital supply voltage	3.3 V	
31	Write Protect output	Low Level : 0V	High Level : 3.3 V
32	Service output	Low Level : 0V	High Level : 3.3 V
33	Reset output	Low Level : 0V	High Level : 3.3 V
34	6 MHz cristal connection 2	Low Level : 0V	High Level : 3.3 V
35	6 MHz cristal connection 1	Low Level : 0V	High Level : 3.3 V
36	Analogue ground		
37	Analogue supply voltage	2.5 V	
38	OSD-Red output	0.7 Vpp to 1.2 Vpp	
39	OSD-Green output	0.7 Vpp to 1.2 Vpp	
40	OSD-Blue output	0.7 Vpp to 1.2 Vpp	
41	OSD-Blanking output	Low Level : 0V	High Level : 3.3 V
42	Digital supply voltage	2.5 V	
43	Ground		
44	Digital supply voltage	3.3 V	
45	PAL / SECAM	Low Level : 0V	High Level : 3.3 V
46	Degauss	Low Level : 0V	High Level : 3.3 V
47	Horizontal Trapezoid	Low Level : 0V	High Level : 3.3 V
48	Tilt	Low Level : 0V	High Level : 3.3 V
49	Not used		
50	Micro s. select	Low Level : 0V	High Level : 3.3 V
51	Comb Filter Standard Selection 2	Low Level : 0V	High Level : 3.3 V
52	SVHS Sense	Low Level : 0V	High Level : 3.3 V

16.9. TDA9181: (For models with Comb-filter)



Pin#:
Pin-1 = Cýn=Chrominance input signal
Pin-2 = INPSEL=input switch select input
Pin-3 =Y/CVBS2=luminance or CVBS input signal 2
Pin-4 = Digital GND
Pin-5= VDD=digital supply voltage
Pin-6=VCC=analog supply voltage
Pin-7 =SC=sandcastle input signal
Pin-8 =FSCSEL=color subcarrier select input
Pin-9 = FSC=color subcarrier input signal
Pin-10 =SYS2=standart select 2 input
Pin-11 = SYS1=standart select 1 input
Pin-12 =Y/CVBS1=luminance or CVBS input signal
Pin-13 = analogue GND
Pin-14 = Y/CVBSout=luminance or CVBS output signal
Pin-15 =OUTSEL=output switch select input
Pin-16 =Cout=chrominance output signal

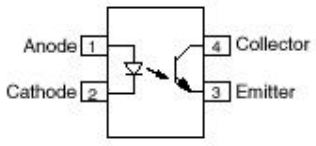
16.9.1. General Features:

-One chip multistandard adaptive comb filter
-Cross luminance reduction
-Cross colour reduction
-No chroma trap, so sharper vertical luminance
-Analogue discrete-time signal processing, so no quantization noise
-Anti aliasing and reconstruction filters are included
-Input switch selects between two Y/CVBS inputs
-Output switch selects between combed CVBS and an external Y/C source
-Fsc as well as 2*fsc colour subcarrier signal may be applied
-Alignment free
-Few external components
-Low power

16.9.2. Limits:

-Analogue supply voltage Vcc=5.5V(max)
-Analogue supply current Icc=25mA(typ)
-Digital supply voltage Vdd=5.5(V)(max)
-Digital supply current Idd=10Ma(typ)
-Luminance or CVBS input signal (p-p) Y/CVBS1, 2 1.4V(max)
-Chrominance input signal (p-p) Cin=1.0V(max)

16.10. TCD1102: (Optocoupler)



16.10.1. Description

The TCET110./ TCET2100/ TCET4100 consists of a phototransistor optically coupled to a gallium arsenide infrared emitting diode in a 4-lead plastic dual inline package. The elements are mounted on one leadframe using a coplanar technique, providing a fixed distances between input and output for highest safety requirements.

16.10.2. Applications

Circuits for safe protective separation against electrical shock according to safety class II (reinforced isolation):
For appl. class I – IV at mains voltage ? 300 V
For appl. class I – III at mains voltage ? 600 V
according to VDE 0884, table 2, suitable for:
Switch-mode power supplies, line receiver, computer peripheral interface, microprocessor system interfaces.

VDE 0884 related features:
Rated impulse voltage (transient overvoltage) V_{IOTM} = 8 kV peak
Isolation test voltage (partial discharge test voltage) V_{pd} = 1.6 kV
Rated isolation voltage (RMS includes DC) V_{IOWM} = 600 V_{RMS} (848 V peak)
Rated recurring peak voltage (repetitive) V_{IORM} = 600 V_{RMS}

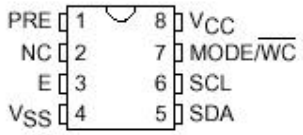
16.10.3. General features:

CTR offered in 9 groups
Isolation materials according to UL94-VO
Pollution degree 2 (DIN/VDE 0110 / resp. IEC 664)
Climatic classification 55/100/21 (IEC 68 part 1)
Special construction: Therefore, extra low coupling capacity of typical 0.2 pF, high **C**ommon **M**ode **R**ejection
Low temperature coefficient of CTR
G = Leadform 10.16 mm; provides creepage distance > 8 mm, for TCET2100/ TCET4100 optional; suffix letter 'G' is not marked on the optocoupler
Coupling System U

16.11. ST24C08:

16.11.1. General description:

The ST24C08 is an 8Kbit electrically erasable programmable memory (EEPROM), organised as 4 blocks of 256 * 8 bits.
The memory operates with a power supply value as low as 2.5V. Both Plastics Dual-in-Line and Plastic Small Outline packages are available.

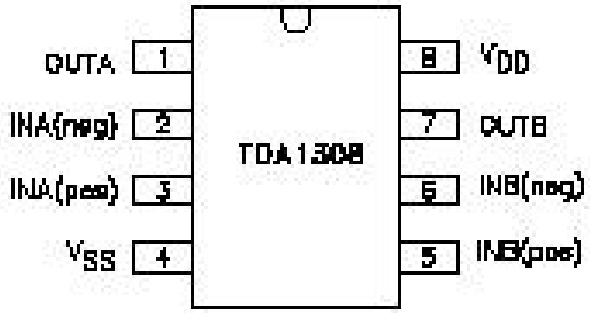


16.11.2. Features:

Minimum 1 million ERASE/WRITE cycles with over 10 years data retention
Single supply voltage:4.5 to 5.5V
Two wire serial interface, fully I2C-bus compatible
Byte and Multibyte write (up to 8 bytes)
Page write (up to 16 bytes)
Byte, random and sequential read modes
Self timed programming cycle

PINNING		PIN VALUE
1. Write protect enable (Ground)	:	0V
2. Not connected (Ground)	:	0V
3. Chip enable input (Ground)	:	0V
4. Ground	:	0V
5. Serial data address input/output	:	Input LOW voltage : Min : -0.3V, Max : 0.3*Vcc Input HIGH voltage: Min : 0.7*Vcc, Max : Vcc+1
6. Serial clock	:	Input LOW voltage : Min: -0.3V, Max : 0.3*Vcc Input HIGH voltage: Min : 0.7*Vcc, Max : Vcc+1
7. Multibyte/Page write mode	:	Input LOW voltage : Min: -0.3V, Max :0.5V Input HIGH voltage: Min : Vcc-0.5, Max : Vcc+1
8. Supply voltage	:	Min : 2.5V, Max : 5.5V

16.12. TDA1308: (Headphone IC)



16.12.1. Features:

Wide temperature range
No switch ON/OFF clicks
Excellent power supply ripple rejection
Low power consumption
Short-circuit resistant
High performance
- high signal-to-noise ratio
- high slew rate
- low distortion

Large output voltage swing

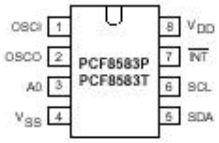
PINNING		PIN VALUE
1. Output A (Voltage swing)	:	Min : 0.75V, Max : 4.25V
2. Inverting input A	:	Vo(clip) : Min : 1400mVrms
3. Non-inverting input A	:	2.5V
4. Ground	:	0V
5. Non-inverting input B	:	2.5V
6. Inverting input B	:	Vo(clip) : Min : 1400mVrms
7. Output B (Voltage swing)	:	Min : 0.75V, Max : 4.25V
8. Positive supply	:	5V, Min : 3.0V, Max : 7.0V

16.13. PCF8583: (Clock IC)

16.13.1. FEATURES

I²C-bus interface operating supply voltage: 2.5 V to 6 V
Clock operating supply voltage (0 to +70 ? C):1.0 V to 6.0 V
240 8-bit low-voltage RAM
Data retention voltage: 1.0 V to 6 V
Operating current (at f_{SCL} = 0 Hz): max. 50 ? A

Clock function with four year calendar
Universal timer with alarm and overflow indication
24 or 12 hour format
32.768 kHz or 50 Hz time base
Serial input/output bus (I 2 C)
Automatic word address incrementing
Programmable alarm, timer and interrupt function
Slave address:
– READ: A1 or A3
– WRITE: A0 or A2.



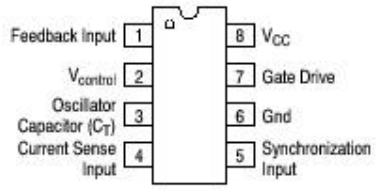
16.13.2. GENERAL DESCRIPTION

The PCF8583 is a clock/calendar circuit based on a 2048-bit static CMOS RAM organised as 256 words by 8 bits. Addresses and data are transferred serially via the two-line bi-directional I²C-bus. The built-in word address register is incremented automatically after each written or read data byte. Address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space. The remaining 240 bytes are free RAM locations.

SYMBOL PIN DESCRIPTION

OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
A0	3	address input
VSS	4	negative supply
SDA	5	serial data line
SCL	6	serial clock line
INT	7	open drain interrupt output (active LOW)
VDD	8	positive supply

16.14. MC33260: (For models with PFC)



16.14.1. General Features:

-Standard Constant Output Voltage or "Follower Boost" Mode
-Switch Mode Operation: Voltage Mode
-Latching PWM for Cycle–by–Cycle On–Time Control
-Constant On–Time Operation That Saves the Use of an Extra Multiplier
-Totem Pole Output Gate Drive
-Undervoltage Lockout with Hysteresis
-Low Start–Up and Operating Current

-Improved Regulation Block Dynamic Behaviour
-Synchronisation Capability
-Internally Trimmed Reference Current Source

16.14.2. Safety Features:

-Overvoltage Protection: Output Overvoltage Detection
-Undervoltage Protection: Protection Against Open Loop
-Effective Zero Current Detection
-Accurate and Adjustable Maximum On–Time Limitation
-Overcurrent Protection
-ESD Protection on Each Pin

16.14.3. LIMITS:

-Vcc MAX voltage 16V
-Gate drive current source=-500mA, sink=500mA
-Input voltage –0.3V to +1.0V
-Operating junction Temperature +150 C

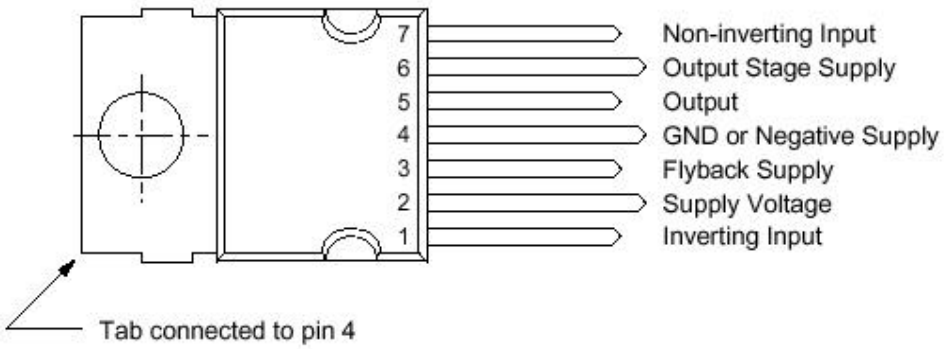
16.14.4. PINNING

Pin1=Feedback input
Pin2=Vcontrol
Pin3=Oscillator capacitor(Ct)
Pin4=Current Sense Input
Pin5=Synchronization Input
Pin6=GND
Pin7=Gate Drive
Pin8=Vcc

16.15. STV9379:

16.15.1. DESCRIPTION

Designed for monitors and high performance TVs, the STV9379FA vertical deflection booster can handle flyback voltage up to 90V. Further to this, it is possible to have a flyback voltage, which is more than the double of the supply (Pin 2). This allows to decrease the power consumption, or to decrease the flyback time for a given supply voltage.
The STV9379FA operates with supplies up to 42V and provides up to 2.6A$_{PP}$ output current to drive the yoke.
The STV9379FA is offered in HEPTAWATT package.

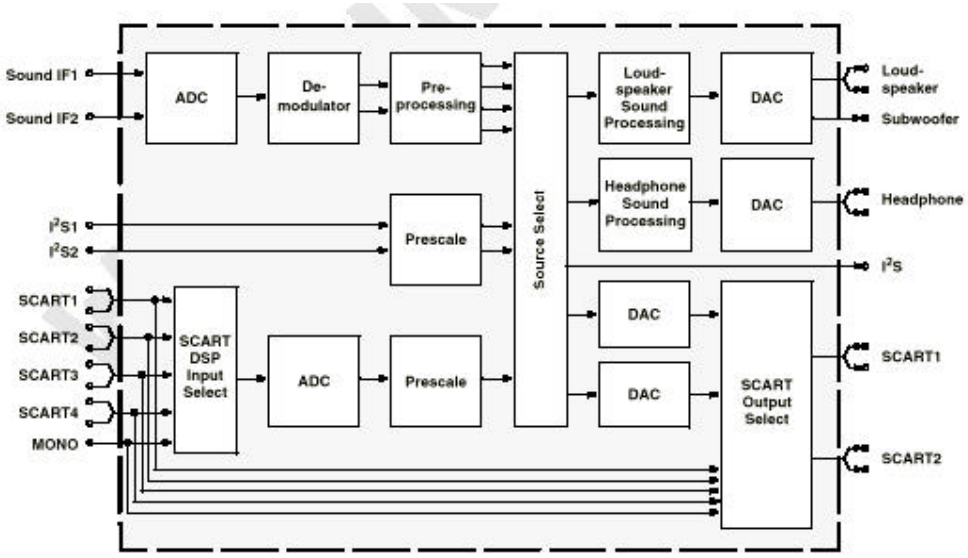


16.15.2. PINNING

Pin1 : Output Stage Supply
Pin2 : Output
Pin3 : GND or Negative Supply
Pin4 : Flyback Supply
Pin5 : Supply Voltage
Pin6 : Inverting Input
Pin7 : Non-inverting Input

16.16. MSP34XX :

MSP3411D
Multistandard Sound Processor Family with Virtual Dolby Surround
1. Introduction
The MSP 34x1G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure shows a simplified functional block diagram of the MSP 34x1G. The MSP 34x1G has all functions of the MSP 34x0G with the addition of a virtual surround sound feature. Surround sound can be reproduced to a certain extent with two loudspeakers. The MSP 34x1G includes our virtualizer algorithm “3D-PANORAMA” which has been approved by the Dolby 1) Laboratories for compliance with the "Virtual Dolby Surround" technology. In addition, the MSP 34x1G includes our “PANORAMA” algo-rithm. These TV sound processing ICs include versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC).
The DBX noise reduction, or alternatively, MICRONAS Noise Reduction (MNR) is performed alignment free. Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.
Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x1G has optimum stereo performance without any adjustments. All MSP 34x1G versions are pin and software downward compatible to the MSP 34x0D. The MSP 34x1G further simplifies controlling software. Standard selection requires a single I 2 C transmission only. The MSP 34x1G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/ stereo/bilingual; no I 2 C interaction is necessary (Automatic Sound Selection).



Source Select

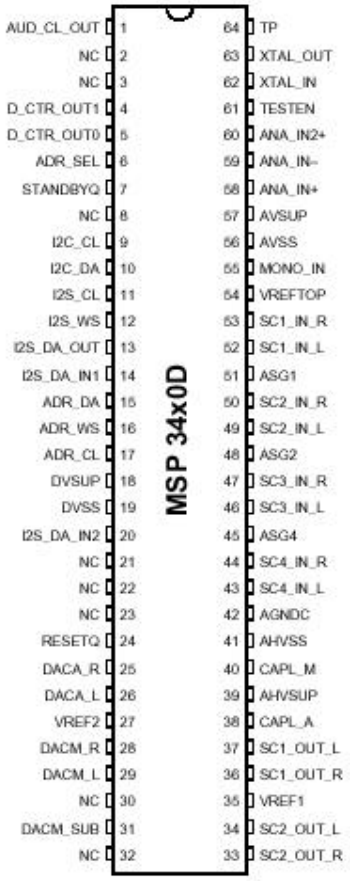
I2S bus interface consists of five pins:

I2S_DA_IN1…2	for input four channels (two channels per line) per sampling cycle (32Khz).
I2DA_OUT,	for output, two channels per sampling cycle (32KHz).
I2S_CL,	for timing of the transmission of I2S serial data, 1.024Mhz.
I2S_WS,	for the word strobe line defining the left and right sample.

Features:

- 5-band graphic equalizer (as in MSP3400C)
- Enhanced spatial affect (pseudo stereo / base-width enlargement as in MSP3400C)
- Headphone channel with balance, bass treble, loudness
- Balance for loudspeaker and headphone channels in dB units (optional)
- Additional pair of D/A converters for SCART2 out
- Improved over-sampling filters (as in MSP 3400C)
- Additional SCART input
- Full SCART in/out matrix without restrictions
- SCART volume in dB units (optional)
- Additional I²S input (as in MSP 3400C)
- New FM-identification (as in MSP 3400C)
- Demodulator short programming
- Auto-detection for terrestrial TV-sound standards
- Precise bit-error rate indication
- Automatic switch from NICAM to FM/AM or vice versa
- Improved NICAM synchronisation algorithm
- Improved carrier mute algorithm
- Improved AM-demodulation
- Reduction of necessary controlling
- Less external components
- Significant reduction of radiation
- 3D-PANORAMA virtualizer (approved by Dolby Laboratories) with noise generator
- PANORAMA virtualizer algorithm
- Standard Selection with single I 2 C transmission
- Automatic Standard Detection of terrestrial TV standards
- Automatic Sound Selection (mono/stereo/bilingual), new registers MODUS, STATUS
- Two selectable sound IF (SIF) inputs
- Automatic Carrier Mute function
- Interrupt output programmable (indicating status change)

- Loudspeaker / Headphone channel with volume, balance, bass, treble, loudness
- AVC: Automatic Volume Correction
- Subwoofer output with programmable low-pass and complementary high-pass filter
- 5-band graphic equalizer for loudspeaker channel
- Spatial effect for loudspeaker channel; processing of all deemphasis filtering
- Four Stereo SCART (line) inputs, one Mono input; two Stereo SCART outputs
- Complete SCART in/out switching matrix
- Two I²S inputs; one I²S output
- All analog FM-Stereo A2 and satellite standards; AM-SECAM L standard
- Simultaneous demodulation of (very) high-deviation FM-Mono and NICAM
- Adaptive deemphasis for satellite (Wegener-Panda, acc. to ASTRA specification)
- ASTRA Digital Radio (ADR) together with DRP 3510A
- All NICAM standards
- Korean FM-Stereo A2 standard



Pinning:

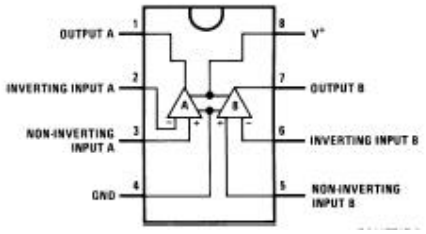
1. ADR wordstrobe
2. Not connected
3. ADR data output
4. I²S 1 data input
5. I²S data output
6. I²S wordstrobe
7. I²S clock
8. I²S data
9. I²S clock
10. Not connected
11. Standby (low-active)
35. Analog Shield Ground 1
36. Scart input 3 in right
37. Scart input 3 in left
38. Analog Shield Ground 4
39. Scart input 4 in, right
40. Scart input 4 in, left
41. Not connected
42. Analog reference voltage high voltage part
43. Analog ground
44. Volume capacitor MAIN
45. Analog power supply 8.0V

12. I²C Bus address select
13. Digital control output 0
14. Digital control output 1
15. Not connected
16. Not connected
17. Not connected
18. Audio clock output
19. Not connected
20. Crystal oscillator
21. Crystal oscillator
22. Test Pin
23. IF input 2 (if ANA_IN1+is used only, connect 50 pF capacitor)
24. IF common
25. IF input 1
26. Analog power supply +5V
27. Analog ground
28. Mono input
29. Reference voltage IF A/D converter
30. Scart input 1 in, right
31. Scart input 1 in, left
32. Analog Shield Ground 2
33. Scart input 2 in, right
34. Scart input 2 in, left
46. Volume capacitor AUX
47. Scart output 1, left
48. Scart output 1, right
49. Reference ground 1 high voltage part
50. Scart output 2, left
51. Scart output 2, right
52. Analog Shield Ground 3
53. Not connected
54. Not connected
55. Not connected
56. Analog output MAIN, left
57. Analog output MAIN, right to AVSS with
58. Reference ground 2 high voltage part
59. Analog output AUX, left
60. Analog output AUX, right
61. Power-on-reset
62. Not connected
63. Not connected
64. Not connected
65. I²S2-data input
66. Digital ground
67. Digital power supply +5V
68. ADR clock

16.17. LM358N: (For rotation circuitry in Real Flat models)

16.17.1. General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits, which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage, which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.



16.17.2. Unique Characteristics

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
The unity gain cross frequency is temperature compensated.
The input bias current is also temperature compensated.

16.17.3. Advantages

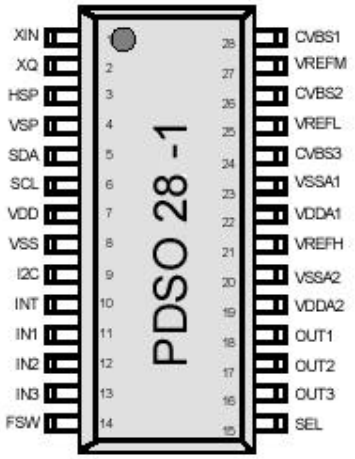
Two internally compensated op amps
Eliminates need for dual supplies
Allows direct sensing near GND and V_{OUT} also goes to GND
Compatible with all forms of logic
Power drain suitable for battery operation
Pin-out same as LM1558/LM1458 dual op amp

16.17.4. Features

Internally frequency compensated for unity gain and large dc voltage gain: 100 dB

Wide bandwidth (unity gain): 1 MHz (temperature compensated)
Wide power supply range:
— Single supply: 3V to 32V
— or dual supplies: ±1.5V to ±16V
Very low supply current drain (500 µA) —essentially independent of supply voltage
Low input offset voltage: 2 mV
Input common-mode voltage range includes ground
Differential input voltage range equal to the power supply voltage
Large output voltage swing: 0V to V + þ 1.5V

16.18. SDA9488x (For models with PIP)



16.18.1. Features

• Single chip solution:
– CVBS-clamping, AD-conversion, gain control (AGC), multistandard chroma decoding, sync separation for inset channel, filtering, embedded memory, RGB-matrix, DA-conversion, RGB / YUV switch, data-slicer and clock generation integrated onto one chip
• Analog inputs:
– 3x CVBS or 1x CVBS and 1x Y/C alternatively
– ADC with 8 bit amplitude resolution
– Automatic Gain Control (AGC)
• Chroma Decoder:
– PAL B/G, PAL M, PAL N(Argentina), PAL60, NTSC M, NTSC4.4 and SECAM
– Adjustable Chroma Saturation and Hue Control
– Automatic Chroma Control (-24 dB ... +6 dB))
– Automatic recognition of 625 lines / 525 lines standard
– Automatic recognition of chroma standards: different search strategies selectable
– Only one crystal necessary for all standards
– IF-characteristic compensation filter
• Display features:
– Horizontal and vertical filtering dependent on picture size
– 7 bit per pixel stored in memory
– PIP sizes between 1/81 and 1/4
– Two 'split-screen' modes with horizontal decimation of 2 and vertical of 1.5 or 1.0
– Resolution up to 324 luminance and 2x81 chrominance pixels per inset line
– 16:9 compatibility
– Field and frame mode display (even at 100/120 Hz with picture sizes<=1/9)
–POP display

– Up to 12 pictures of 1/36th size (11 still and 1 moving)
– Up to 6 pictures of 1/16th size (5 still and 1 moving)
– Up to 3 pictures of 1/9th size (2 still and 1 moving)
– Jointline free display
– Display on VGA and SVGA screen (f H limited to 40kHz)
– Line doubling mode for progressive scan applications
• Zoom:
– Fine variation of picture size(steps of 4 pixel / 2 lines)
• Wipe in / Wipe out capability:
– 3 time periods programmable
• Programmable position of inset picture:
– Coarse positioning at 4 corners of the parent picture
– Fine positioning at steps of 4 pixels and 2 lines
• Freeze picture

Pin No:	Name	Short Description
1	XIN	crystal oscillator (input) or crystal clock (from another IC)
2	XQ	crystal oscillator (output)
3	HSP	horizontal sync for parent channel
4	VSP	vertical sync for parent channel
5	SDA	I²C-bus data
6	SCL	I²C-bus clock
7	VDD	digital supply voltage
8	VSS	digital ground
9	I²C	I²C Address
10	INT	interrupt
11	IN1	V/R Input for external YUV/RGB source
12	IN2	Y/G Input for external YUV/RGB source
13	IN3	U/B Input for external YUV/RGB source
14	FSW	fast switch input for YUV/RGB switch
15	SEL	fast blanking output for PIP
16	OUT3	analog output: chrominance signal +(B-Y) or -(B-Y) or B
17	OUT2	analog output: luminance signal Y or G
18	OUT1	analog output: chrominance signal +(R-Y) or -(R-Y) or R
19	VDDA2	analog supply voltage (V DDA) for DAC
20	VSSA2	analog ground (V SS) for DAC
21	VREFH	reference voltage for ADC and DAC (high)
22	VDDA1	analog supply voltage (V DDA) for ADC
23	VSSA1	Analog ground (Vss) for ADC
24	CVBS3	CVBS Input 3 or C (selectable via I²C-bus)
25	VREFL	Reference voltage for ADC (low)
26	CVBS2	CVBS Input 2 or Y (selectable via I²C-bus)
27	VREFM	Reference voltage for ADC(medium)
28	CVBS1	CVBS Input 1 (selectable via I²C-bus)

16.19. TDA9885I (For models with PIP)

5 V supply voltage
Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier (AC-coupled)
Multistandard true synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
Gated phase detector for L/L accent standard
Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free; frequencies switchable for all negative and positive modulated standards via I²C-bus
Digital acquisition help, VIF frequencies of 33.4, 33.9, 38.0, 38.9, 45.75 and 58.75 MHz

4 MHz reference frequency input [signal from Phase-Locked Loop (PLL) tuning system] or operating as crystal oscillator

VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals

Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter; AFC bits via I²C-bus readable

TakeOver Point (TOP) adjustable via I²C-bus or alternatively with potentiometer

Fully integrated sound carrier trap for 4.5, 5.5, 6.0 and 6.5 MHz, controlled by FM-PLL oscillator

Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode (PLL controlled)

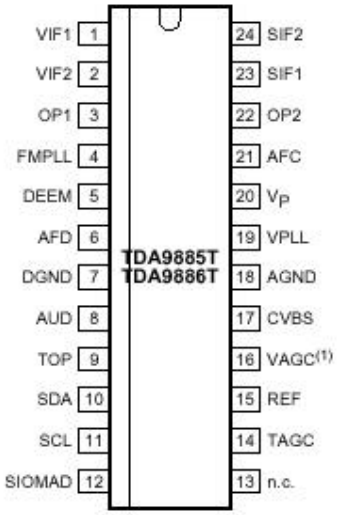
SIF AGC for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I²C-bus

AM demodulator without extra reference circuit

Alignment-free selective FM-PLL demodulator with high linearity and low noise

I²C-bus control for all functions

I²C-bus transceiver with pin programmable Module Address (MAD).



GENERAL DESCRIPTION

The TDA9885 is an alignment-free single standard (without positive modulation) vision and sound IF signal PLL.

The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation including sound AM and FM processing.

Pin No:	Name	Short Description
1	VIF1	VIF differential input 1
2	VIF2	VIF differential input 2
3	OP1	output 1 (open-collector)
4	FMPLL	FM-PLL for loop filter
5	DEEM	de-emphasis output for capacitor
6	AFD	AF decoupling input for capacitor
7	DGND	digital ground
8	AUD	audio output
9	TOP	tuner AGC TakeOver Point (TOP)
10	SDA	I²C-bus data input/output
11	SCL	I²C-bus clock input
12	SIOMAD	sound intercarrier output and MAD select
13	NC	not connected
14	TAGC	tuner AGC output
15	REF	4 MHz crystal or reference input
16	VAGC	VIF-AGC for capacitor

17	CVBS	video output
18	AGND	analog ground
19	VPLL	VIF-PLL for loop filter
20	VP	supply voltage (+5 V)
21	AFC	AFC output
22	OP2	output 2 (open-collector)
23	SIF1	SIF differential input 1
24	SIF2	SIF differential input 2

17. CHASSIS MANUAL ADJUSTMENTS PROCEDURE

In order to enter the service menu, first enter the installation menu (blue button on the remote control) and then press the digits 4, 7, 2 and 5 respectively.

For ADJUST settings:

Select **Adjust** using or button and press < or > button to enter it. To select different adjust parameters , use or button. To change the selected parameter, you should use < or > button.

ADJUST LIST

ADJUST 00	=	White Point RED
ADJUST 01	=	White Point GREEN
ADJUST 02	=	White Point BLUE
ADJUST 03	=	AGC
ADJUST 04	=	IF-PLL Negative
ADJUST 05	=	IF-PLL Positive
ADJUST 06	=	Y-Delay PAL
ADJUST 07	=	Y-Delay SECAM
ADJUST 08	=	Y-Delay NTSC
ADJUST 09	=	Y-Delay OTHER
ADJUST 10	=	4:3 Vertical Zoom
ADJUST 11	=	4:3 Vertical Scroll
ADJUST 12	=	4:3 Horizontal Shift
ADJUST 13	=	4:3 Vertical Slope
ADJUST 14	=	4:3 Vertical Amplitude
ADJUST 15	=	4:3 S-correction
ADJUST 16	=	4:3 Vertical Shift
ADJUST 17	=	4:3 EW Width
ADJUST 18	=	4:3 EW Parabola Width
ADJUST 19	=	4:3 EW Upper Corner Parabola
ADJUST 20	=	4:3 EW Trapezium
ADJUST 21	=	4:3 Horizontal Parallelogram
ADJUST 22	=	4:3 Bow
ADJUST 23	=	4:3 EW Lower Corner Parabola
ADJUST 24	=	16:9 Vertical Zoom
ADJUST 25	=	16:9 Vertical Scroll
ADJUST 26	=	16:9 Horizontal Shift
ADJUST 27	=	16:9 Vertical Slope
ADJUST 28	=	16:9 Vertical Amplitude
ADJUST 29	=	16:9 S-correction
ADJUST 30	=	16:9 Vertical Shift

ADJUST 31	=	16:9 EW Width
ADJUST 32	=	16:9 EW Parabola Width
ADJUST 33	=	16:9 EW Upper Corner Parabola
ADJUST 34	=	16:9 EW Trapezium
ADJUST 35	=	16:9 Horizontal Parallelogram
ADJUST 36	=	16:9 Bow
ADJUST 37	=	16:9 EW Lower Corner Parabola
ADJUST 38	=	Cinema Vertical Zoom
ADJUST 39	=	Cinema Vertical Scroll
ADJUST 40	=	Cinema Horizontal Shift
ADJUST 41	=	Cinema Vertical Slope
ADJUST 42	=	Cinema Vertical Amplitude
ADJUST 43	=	Cinema S-correction
ADJUST 44	=	Cinema Vertical Shift
ADJUST 45	=	Cinema EW Width
ADJUST 46	=	Cinema EW Parabola Width
ADJUST 47	=	Cinema EW Upper Corner Parabola
ADJUST 48	=	Cinema EW Trapezium
ADJUST 49	=	Cinema Horizontal Parallelogram
ADJUST 50	=	Cinema Bow
ADJUST 51	=	Cinema EW Lower Corner Parabola
ADJUST 52	=	Subtitle Vertical Zoom
ADJUST 53	=	Subtitle Vertical Scroll
ADJUST 54	=	Subtitle Horizontal Shift
ADJUST 55	=	Subtitle Vertical Slope
ADJUST 56	=	Subtitle Vertical Amplitude
ADJUST 57	=	Subtitle S-correction
ADJUST 58	=	Subtitle Vertical Shift
ADJUST 59	=	Subtitle EW Width
ADJUST 60	=	Subtitle EW Parabola Width
ADJUST 61	=	Subtitle EW Upper Corner Parabola
ADJUST 62	=	Subtitle EW Trapezium
ADJUST 63	=	Subtitle Horizontal Parallelogram
ADJUST 64	=	Subtitle Bow
ADJUST 65	=	Subtitle EW Lower Corner Parabola
ADJUST 66	=	Zoom Vertical Zoom
ADJUST 67	=	Zoom Vertical Scroll
ADJUST 68	=	Zoom Horizontal Shift
ADJUST 69	=	Zoom Vertical Slope
ADJUST 70	=	Zoom Vertical Amplitude
ADJUST 71	=	Zoom S-correction
ADJUST 72	=	Zoom Vertical Shift
ADJUST 73	=	Zoom EW Width
ADJUST 74	=	Zoom EW Parabola Width
ADJUST 75	=	Zoom EW Upper Corner Parabola
ADJUST 76	=	Zoom EW Trapezium
ADJUST 77	=	Zoom Horizontal Parallelogram
ADJUST 78	=	Zoom Bow
ADJUST 79	=	Zoom EW Lower Corner Parabola
ADJUST 80	=	OSD position
ADJUST 81	=	Tilt
ADJUST 82	=	Trapezoid

WHITE BALANCE ADJUSTMENT:
The following three parameters are used to make white balance adjustment. To do this, use a Colour Analyser. Using white point RED, white point GREEN and white point BLUE parameters, insert the + sign in the square which is in the middle of the screen.

ADJUST 00 = White Point RED
ADJUST 01 = White Point GREEN
ADJUST 02 = White Point BLUE

These adjustments' factory settings are 026, 026, 030 respectively.

AGC ADJUSTMENT:
ADJUST 03 = AGC
In order to do AGC adjustment, enter a 60dBmV RF signal level from channel C-12.
Connect a digital voltmeter to pin 1 of the tuner. Change the AGC parameter until you see 3.10 Vdc on voltmeter display. Check that picture is normal at 90dBmV signal level.

IF-PLL NEGATIVE ADJUSTMENT
ADJUST 04 = IF-PLL Negative

Connect 38.9 MHz test pattern for PAL B/G, PAL-SECAM B/G, 39.5 MHz test pattern for PAL I or 45.75 MHz test pattern for PAL M/N, NTSC M model to Z201 SAW filter input terminals. Change the IF-PLL Negative parameter until you see IN, DOWN below the Adjustment OSD. This adjustment's factory setting is 080.

IF-PLL POSITIVE ADJUSTMENT:
ADJUST 05 = IF-PLL Positive
Connect 33.9 MHz test pattern for SECAM L' model to Z201 SAW filter input terminals. Change the IF-PLL Positive parameter until you see IN, DOWN below the Adjustment OSD. This adjustment's factory setting is 080.

LUMINANCE DELAY ADJUSTMENT:
ADJUST 06 = Y-Delay PAL
Enter a PAL B/G colour and black-white bar test pattern via RF. Adjust Y-Delay PAL till the colour transients on the colour bar of the pattern become as sharp as possible and colours between transients do not mix with each other. This adjustment's factory setting is 008.

ADJUST 07 = Y-Delay SECAM
Enter a SECAM B/G colour and black-white bar test pattern via RF. Adjust Y-Delay SECAM till the colour transients on the colour bar of the pattern become as sharp as possible and colours between transients do not mix with each other. This adjustment's factory setting is 011.

ADJUST 08 = Y-Delay NTSC
Enter an NTSC colour and black-white bar test pattern via RF. Adjust Y-Delay NTSC till the colour transients on the colour bar of the pattern become as sharp aaas possible and colours between transients do not mix with each other. This adjustment's factory setting is 012.

ADJUST 09 = Y-Delay Other
In case of other colour systems, enter this system with colour and black-white bar test pattern via RF. Adjust Y-Delay Other till the colour transients on the colour bar of the pattern become as sharp as possible and colours between transients do not mix with each other. Normally for an equal delay of the luminance and chrominance signal the delay must be set at a value of 160nS. This adjustment's factory setting is 007.

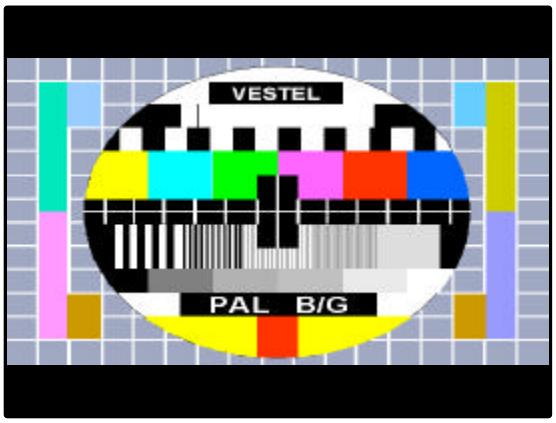
GEOMETRY ADJUSTMENTS:

These adjustments are used to get a proper picture geometry in different picture modes: 4/3, 16/9, Cinema (Subtitle and Zoom are optional picture modes)

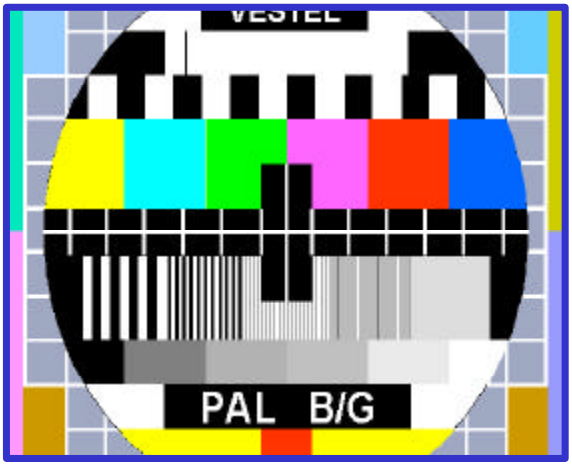
After these adjustments the geometry must be like the ones shown below :

4:3 mode for 4:3 CRTs

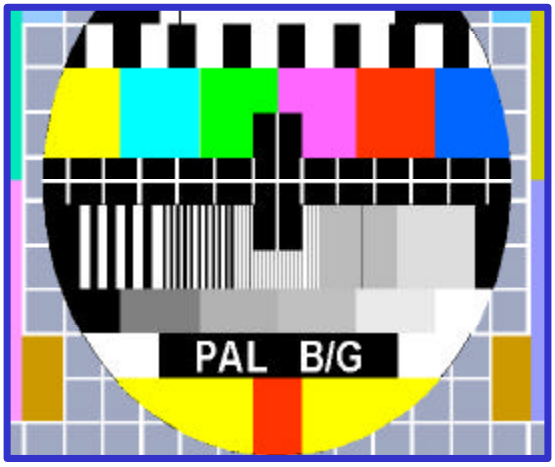
16 : 9 mode for 4:3 CRTs



Cinema mode for 4:3 CRTs

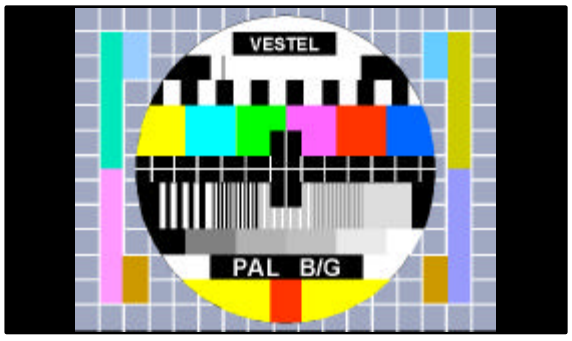


Subtitle mode for 4:3 CRTs

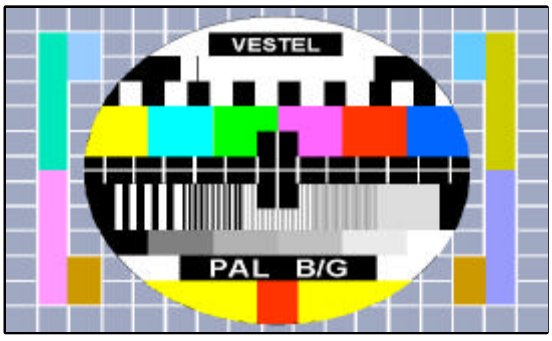


Zoom mode for 4:3 CRTs

4: 3 mode for 16:9 CRTs



16: 9 mode for 16:9 CRTs



Cinema mode for 16: 9 CRTs

Subtitle mode for 16: 9 CRTs

Zoom mode for 16: 9 CRTs

4:3 VERTICAL ZOOM ADJUSTMENT:
ADJUST 10 = Vertical Zoom
Enter a PAL B/G circle test pattern via RF. Change vertical zoom till you see the upper and lower limit of the circle as close to the upper and lower limit of the picture tube as possible.

4:3 VERTICAL SCROLL ADJUSTMENT:
ADJUST 11 = Vertical Scroll
Enter a PAL B/G circle test pattern via RF. Change vertical scroll till you see the circle exactly in the middle of the screen.

4:3 HORIZONTAL SHIFT ADJUSTMENT:
ADJUST 12 = 4 : 3 Horizontal Shift
Enter a RED PURITY test pattern via RF. Change horizontal shift till the picture is horizontally centred. Check whether this adjustment is correct after completing Service Mode Adjustment.

4:3 VERTICAL SLOPE ADJUSTMENT:
ADJUST 13 = 4 : 3 Vertical Slope
Enter a CROSS-HATCH B/G test pattern via RF. Change vertical slope till the size of squares on both the upper and lower part of test pattern become equal to the squares laying on the vertical centre of the test pattern. Check and readjust VERTICAL SLOPE item if the adjustment becomes improper after some other geometric adjustments are done.

4:3 VERTICAL AMPLITUDE ADJUSTMENT:
ADJUST 14 = 4 : 3 Vertical Amplitude
Enter a PAL B/G test pattern via RF. Change vertical slope till horizontal black lines on both the upper and lower part of the test pattern become very close to the upper and lower horizontal sides of picture tube and nearly about to disappear. Check and readjust VERTICAL AMPLITUDE item if the adjustment becomes improper after some other geometric adjustments are done.

4:3 S-CORRECTION ADJUSTMENT:
ADJUST 15 = 4 : 3 S-Correction
Enter a PAL B/G circle test pattern via RF. Change S-correction till the middle part of the circle is as round as possible.

4:3 VERTICAL SHIFT ADJUSTMENT:
ADJUST 16 = 4 : 3 Vertical Shift
Enter a PAL B/G test pattern via RF. Change Vertical Shift till the test pattern is vertically centred, i.e. horizontal line at the centre pattern is in equal distance both to upper and lower side of the picture tube. Check and readjust Vertical Shift item if the adjustment becomes improper after some other geometric adjustments are done.

4:3 EW WIDTH ADJUSTMENT (only for 110° picture tubes):
ADJUST 17 = 4 : 3 EW Width
Enter a PAL B/G test pattern via RF. Change EW Width till the vertical black and white bars on both left and right side of the pattern exactly disappear.

4:3 EW PARABOLA WIDTH ADJUSTMENT (only for 110° picture tubes):
ADJUST 18 = 4 : 3 EW Parabola Width
Enter a PAL B/G test pattern via RF. Change EW Parabola Width till vertical lines close to the both sides of the picture frame become parallel to vertical sides of picture tube. Check and readjust EW Parabola Width item if the adjustment becomes improper after some other geometric adjustments are done.

4:3 EW UPPER CORNER PARABOLA ADJUSTMENT (only for 110° picture tubes):
ADJUST 19 = 4 : 3 EW Corner Parabola
Enter a PAL B/G test pattern via RF. Change EW Upper Corner Parabola till vertical lines at the corners of both sides of picture frame become vertical and parallel to vertical corner sides of picture tube. Check and readjust EW Upper Corner Parabola item if the adjustment becomes improper after some other geometric adjustments are done.

4:3 EW TRAPEZIUM ADJUSTMENT:
ADJUST 20 = 4 : 3 EW Trapezium
Enter a PAL B/G test pattern via RF. Change EW Trapezium till vertical lines, especially lines at the sides of the picture frame became parallel to the both sides of picture tube as close as possible. Check and readjust EW Trapezium item if the adjustment becomes improper after some other geometric adjustments are done.

4:3 HORIZONTAL PARALLELOGRAM:
ADJUST 21 = Horizontal Parallelogram
Enter a PAL B/G test pattern via RF. Change Horizontal Parallelogram to set vertical lines orthogonal to the horizontal lines Check and readjust Horizontal Parallelogram item if the adjustment becomes improper after some other geometric adjustments are done.

4:3 BOW:
ADJUST 22 = Bow
Enter a PAL B/G test pattern via RF. Change Bow to straighten the vertical lines. Check and readjust Bow item if the adjustment becomes improper after some other geometric adjustments are done.

4:3 EW LOWER CORNER PARABOLA ADJUSTMENT (only for 110° picture tubes):
ADJUST 23 = 4 : 3 EW Lower Corner Parabola
Enter a PAL B/G test pattern via RF. Change EW Lower Corner Parabola till vertical lines at the corners of both sides of picture frame become vertical and parallel to vertical corner sides of picture tube. Check and readjust EW Lower Corner Parabola item if the adjustment becomes improper after some other geometric adjustments are done.

The adjustments and their functions and the procedures are the same for 16:9, Cinema, Subtitle and Zoom modes. The resultant geometry of the pictures must be like the pictures shown above. The adjustment numbers are given above as a list " Adjustment List".

OSD POSITION:
ADJUST 80 = OSD POSITION
The vertical position of the OSD can be set.

TILT ADJUSTMENT:
ADJUST 81 = TILT ADJUSTMENT

Enter a PAL B/G test pattern via RF. Change TILT till horizontal and vertical lines at the corners of both sides of picture frame become vertical and parallel to vertical corner sides of picture tube. Check and readjust TILT item if the adjustment becomes improper after some other geometric adjustments are done.

TRAPEZOID ADJUSTMENT:
ADJUST 82 = TRAPEZOID ADJUSTMENT
Enter a PAL B/G test pattern via RF. Firstly set the TILT adjustment and then change TRAPEZOID till vertical lines at the corners of lower sides of picture frame become vertical and parallel to vertical corner sides of picture tube. Check and readjust TRAPEZOID item if the adjustment becomes improper after some other geometric adjustments are done.

**note that some adjustments are fixed to default values in order to get correct geometry in all picture modes(4:3,16:9,Cinema,Subtitle,Super zoom)

CIRCUIT DESCRIPTION

(Refer to the Schematic Diagrams while reading this description)

A) POWER SUPPLY

The chassis incorporates a Motorola switch mode power supply using a MC44608 regulator controller IC. The circuit provides power to the receiver in both stand-by and normal operation modes. The DC voltages required at various parts of the chassis are provided by an SMPS transformer controlled by the IC MC44608, which is designed for driving, controlling and protecting switching transistor of SMPS. The transformer produces 150V for FBT input, +/-14V for audio output IC, S+3.3, S+5V , +5V, +3.3V for controller and MSP and 8V for TDA8885.

START UP

The switch on the mains supply is fed through the mains filter network L107 and L108 , the surge limiter resistor R100 , the bridge rectifier diode D132, and reservoir capacitor C116, producing approximately 310Vdc to feed the switching MOSFET Q102 via the primary winding of TR101 pins 3 and 5. This process occurs in models without PFC (Power Factor Correction) circuitry. In models with PFC, the PFC circuitry based on the Motorola IC MC33260 is also effective and an approximately 380Vdc is produced to feed the switching MOSFET Q102. The MC33260 is a controller for Power Factor Correction pre-converters meeting international standard requirements in electronic ballast and off–line power conversion applications. Designed to drive a free frequency discontinuous mode, it can also be synchronised and in any case, it features very effective protections that ensure a safe and reliable operation. The voltage to run the switching MOSFET Q100 is fed through L102 coil and this MOSFET runs MC33260 to run the PFC circuitry.

Start up resistor R101 feeds from a 500V coming from the mains through the adder diodes D104, D135 to pin 8 of IC106 (MC44608), the IC uses 9mA current source and connects it internally to VCC at pin6 allowing a rapid charge enough for start up. Then IC106 responds with the oscillator starting to oscillate at a 40khz frequency fixed by the IC manufacturer.

The IC then produces, pulse width modulation pulses, at this frequency on pin 5 to drive the base of the switching MOSFET Q102, that will then switch current on and off through the primary of TR101, which will in turn provides voltages in the secondary windings. The secondary winding voltages being proportional to the length of time that Q102 is turned on in each cycle. The voltage produced between pins 8 and 9 of TR101 is rectified by D105 developing approx. 12 volts on C110, which takes over from the start up resistor to supply pin 8 of IC106. This voltage is also used for Demag. pin (pin 1) of IC106 and VCC pin (pin 8) of IC 107 (MC33260) .

The Demag. pin at pin1 of IC106 offers 3 different functions: Zero voltage crossing detection (50mV), 24mA current detection and 120mA current detection. The 24mA level is used to detect the secondary reconfiguration status and the 120mA level to detect an Over Voltage status called Quick OVP.

The VCC at pin 6 of IC106 operates between 6,6V and 13V in normal operation, when this voltage exceeds 15V then the IC output is disabled.

VOLTAGE REGULATION

After initial start up, the secondary voltages of TR101 are established. These voltages then need to be regulated to the required levels. In a switch mode power supply such as this, it is the ON time of the switching FET Q102 that determines the output voltages produced. To provide regulation of the supply there is a feedback loop via an adjustable zener IC116 and an OPTO- coupler (IC 100) connected to pin3 of IC106. The reference voltage of IC116 is set to 2,5V to supply a B+ voltage of 115V. Any fluctuation at this pin will cause IC106 to compensate it either by increasing or decreasing the voltage at the secondary outputs.

VOLTAGE PROTECTION

The MC44608 offers two OVP functions:
1- A fixed function that detects when VCC is higher than 15.4V
2- A programmable function that uses the demag pin. The current flowing into the demag pin is mirrored and compared to the reference current Iovp (120mA). -Thus this OVP is quicker than normal number one as it directly sense the change in current rather than waiting for a specific voltage value, and is called QOVP. In both cases, once an OVP condition is detected, the output is latched off until a new circuit START–UP.
3- In the chassis there is also a voltage protection according to a detection of high current over B+ Supply voltage by sensing the current through R144. If the current over R144 is higher then a value arranged for different CRTs (e.g. 1.2 A for 29" RF 4:3 models), then by sensing and by the B+ protection circuitry a voltage is applied to the pin 3 of video processor IC. When the voltage at this pin is higher then 3.4V the TV switches to stand-by mode.
4-Another voltage protection is by the pin 18 of micro-controller. When there appears to be a shortcut between 8V and 5V supplies, through R500 and R501 the shortcut is sensed and pin 18 port gets low and TV turns to stand-by mode. In normal condition, pin 18 is high.

CURRENT PROTECTION

To monitor the current drawn by the receiver the source of Q102 is returned to the bridge rectifier through low value resistor R153, R116 in parallel. All the current drawn by the receiver will flow through those resistors each time Q102 conducts, this will produce a voltage across the resistors proportional to the current drawn by the receiver. This voltage is fed to pin 2 (I-sense) of IC106 via R108. When the receiver is working normally the voltage across R153//R116 is only a fraction of a volt and is not large enough to have any effect on IC106. Under fault conditions, if the receiver draws excessive current the voltage across R153//R116 will rise. This voltage is monitored by the current sense input pin2.

This Current Sense pin senses the voltage developed on the series resistor R108 inserted in the source of the power MOSFET. When I sense reaches 1V, the Driver output (pin 5) is disabled. This is known as the Over Current Protection function. A

200mA current source is flowing out of the pin 3 during the start–up phase and during the switching phase in case of the Pulsed Mode of operation. A resistor can be inserted between the sense resistor and the pin 3. Thus a programmable peak current detection can be performed during the SMPS stand–by mode.

SAFETY PRECAUTIONS

Remember that all the primary side components of the power supply shown to the left of TR101 on the diagram are live to earth. It is recommended that a mains isolation transformer is used when servicing the receiver.
Many of the components in the power supply are safety critical. These are marked with an exclamation mark in a triangle on the circuit diagram. These components MUST be replaced only with parts of identical value and safety characteristics. For reliability, it is recommended that only genuine parts should be used for service replacements. Always check the main supply voltage feeding the line output stage after replacing parts in the power supply or line output circuit. The correct voltage is important for safety and reliability, the correct voltage should be 145V ±2 V. (Only for 29" 4:3 Full RCA tubes this voltage is 150V.)
Additionally, the voltage on reservoir capacitor C116 must be approximately 380V for models with PFC. without PFC option or with spoiled PFC circuitry, this voltage becomes approximately 310V. If you observe 310V but there is PFC circuitry in the chassis, then it means that PFC is out of order. The TV still works; but with no PFC.
When servicing note that the reservoir capacitor C116 can remain charged to high voltage for some time after the AC supply is removed. This can result in a shock hazard or damage to components whilst working on the receiver. Do not try to test Q102 base emitter junction if C116 capacitor is charged, your meter will turn on the transistor that will discharge the capacitor resulting in a collector emitter short circuit. Do not discharge C116 quickly with a screwdriver etc. The very high current produced can damage the internal connections of the capacitor causing failure at a later date. Remember when checking voltages to use a return path on the same side of TR101 for the Voltmeter earth to obtain the correct readings.

All the precautions and responsibilities are done with the new layout designed according to the Japanese standards. The new layout is indicated with J meaning Japanese.

STANDBY OPERATION

As mentioned earlier the Start–up Management of MC44608 is as follows:

The Vi pin 8 of IC106 is directly connected to the HV DC rail Vin. This high voltage current source is internally connected to the VCC pin and thus issued to charge the VCC capacitor. The VCC capacitor charge period corresponds to the Start–up phase. When the VCC voltage reaches 13V, the high voltage 9mA current source is disabled and the device starts working. The device enters into the switching phase.
To help increase the application safety against high voltage spike on pin8 a small wattage 1k _ series resistor is inserted between the Vin rail and pin 8. After this start-up the IC can distinguish between the different modes of operation using the following technique:

MODE TRANSITION

This chassis automatically selects stand-by mode when switched on.(For some special models this case is changed by software, according to the customer requests, such that TV selects the mode which was selected when the TV is turned off, whether directly power-off or first stand-by then power-off)
The concept IC MC44608 is designed to detect the transitions between the stand-by and normal mode and to manage each mode in an optimal way.
In stand-by, the device monitors a pulsed mode that enables to drastically reduce the power consumption.

The LW latch is the memory of the working status at the end of every switching sequence. Two different cases must be considered for the logic at the termination of the SWITCHING PHASE:
1. No Over Current was observed
2. An Over Current was observed
These two cases correspond to the two signals "NOC" in case of "No Over Current" and "OC" in case of Over Current. The effective working status at the end of the ON time memorised in LW corresponds to Q=1 for no over current, and Q=0 for over current.

To enter the standby mode, secondary side is reconfigured using Q107 loop. This starts with the micro-controller's pin 27 becomes high; as the standby port becomes high Q516 conducts and Q105 becomes off, then Q107 conducts and the high voltage output value becomes lower than the NORMAL mode regulated value. The shunt regulator IC116 is fully OFF. In the SMPS stand–by mode all the SMPS outputs are lowered except for the low voltage output that supply the wake–up circuit located at the isolated side of the power supply. In that mode the secondary regulation is performed by the zener diode D123 connected in parallel to the TL431. The secondary reconfiguration status can be detected on the SMPS primary side by measuring the voltage level at pin8 of TR101.
In the SMPS stand–by mode the 3 distinct phases are:

The SWITCHING PHASE: Similar to the Overload mode. The current sense clamping level is reduced. When VCC crosses the current sense section, the C.S. clamping level depends on the power to be delivered to the load during the SMPS stand–by mode. Every switching sequence ON/OFF is terminated by an OC as long as the secondary Zener diode voltage has not been reached. When the Zener voltage is reached the ON cycle is terminated by a true PWM action. The proper SWITCHING PHASE termination must correspond to a NOC condition. The LW latch stores this NOC status.

The LATCHED OFF PHASE: The MODE latch is set.
The START–UP PHASE is similar to the Overload Mode. The MODE latch remains in its set status (Q=1).
The SWITCHING PHASE: The Stand–by signal is validated and the 200uA current comes out of the Current Sense pin 2.

SMPS SWITCH OFF

When the mains is switched OFF, so long as the electrolytic bulk capacitor provides energy to the SMPS the controller remains in the switching phase. Then the peak current reaches its maximum peak value, the switching frequency decreases and all the secondary voltages are reduced. The VCC voltage is also reduced. When VCC is less than 6.5V, the SMPS stops working.

B) MICRO-CONTROLLER IC500

IC 500 controls all the functions of the receiver operated by the remote control and the front panel customer controls. It produces the on screen graphics, operates tuning, customers controls and engineering and servicing controls, and also incorporates all of the Tele-text functions. It also controls the video processor, the audio processor, and the tuner. The circuits just mentioned are controlled via the I²C bus. Also IC501 controls the video source switching, vertical position adjustment and the vertical linearity adjustment via its ports.

An external 8K eeprom is used by the micro. The eeprom comes fully programmed. The main clock oscillator is 6.0 MHz crystal X500 on pins 34 and 35. Reset is provided on pin 33 via Q504. On switching on pin 34 becomes high and the controller gets reset which stays valid till a low signal comes on that pin.

CONTROLS

Command information from the infra red remote controller is fed through the sensor on the keyboard (front panel) in front of the cabinet to pin 24 of the micro-controller. Operations on the customer front panel keys are detected by pin 4,5,6,7 those are ADCs (analogue to digital converter). Pressing a switch will connect the 3.3V to the ground through a particular resistor that makes a voltage on the dedicated pin for that switch at that instant and, so micro-controller detects to operate which function and the corresponding operation is performed.

IC500 automatically switches from TV mode to AV1, AV2 if a source is connected to SCART-connectors, by detecting the signal coming from pin8 of the two SCART-connectors, through pin16 and pin17 respectively.

TUNING

All the tuning functions are carried by the micro-controller IC500. Two tuning modes are available for this chassis PLL tuning and frequency tuning. For both, both manual and automatic modes are possible. If Auto Tuning Mode is selected the receiver tunes Band 1, Band2, and UHF, putting into memory the channel, signal strength (video indent for PLL), and tuning data of each TV station found. The memories are then stored automatically to put the channels into frequency order from lowest frequency to the highest one. In APS (Auto-Programming-System) TV sets the channels are stored according to the standard tables provided for each country.

In both PLL and frequency tuning modes the tuning process is controlled by IC501 via the I²C BUS. In PLL mode a table for all the channels available is set according

to the standards and the micro controller uses these values to set the central frequency of the required channel. This mode is quicker than frequency mode. Frequency tuning is a new feature to this chassis. It takes the advantages of both VST and PLL tuning. As in PLL mode the tuning process is controlled via I²C bus, however the channels are not predefined in the software by a table, on the contrary these are scanned as in VST tuning mode but here the frequency changes, not the voltage. In frequency tuning the micro-controller generates I²C signals to account for a 1Mhz frequency increment on the tuner and then scan all the frequency either manually or automatically. This frequency tuning method is more precise than PLL tunings. Tuner AGC voltage from pin 7 of IC200 is taken directly to the tuner pin 1. This is used in auto tuning.

VOLUME CONTROL

A pulse width modulation output is developed inside the controller and is fed to the audio processor via the I²C BUS to control the volume. The physical control on the front panel works in the same way.

TELETEXT

The micro-controller IC500 performs all of the Tele-text functions internally. The Composite Blanking video and Sync signal (CBVS) is input to pin 12 of the micro-controller from pin 54 of IC200. When text is selected the text graphics are output as R.G.B signals on pins 38/39/40 of the micro and fed to pins 35/36/37 of IC200. At the same time pin 41 of the micro goes high taking pin 38 of IC200 high, blanking the picture and selecting text R.G.B. input. Also in the text mode, pin 20 of micro sends synchronous odd-even signal, to make the odd and even picture rows intersect with each other, by affecting the non-inverted input (pin7) of the vertical IC, IC600.
Note: Mixed mode is available and fast text with 8-page memory.

EEPROM INITIALISATION

If the E²PROM IC502 is replaced, the new one will come fully programmed and therefore it is not necessary to initialise the new device. In some circumstances the E²PROM may become corrupted in use, i.e. static discharge or lightning strike. If this happens, it is advised to replace the E²PROM.

C) OFF AIR SIGNAL PATH

TUNER

A UV1315 voltage controlled tuner is used on this chassis, operating from a 5 volt supply, line (pin7). 0 to 33 volt rail is used for tuning (pin 9), controlled by the microprocessor IC501. This is done by software in IC501. The gain of the tuner can be altered by AGC control voltage fed in to pin1. The tuner produces a balanced output on pins 10,11. Neither side is connected to earth. This is fed via a surface wave filter Z201 to the IF input of IC200 (pins 1 and 2). The same IF signals are also fed via surface wave (SAW) filter Z200 to the Sound-IF input of IC200 (pins 8 and 9). IC200 incorporate the IF amplification, AGC, video and sound detectors.

VIDEO PATH

In this chassis the TDA 8885 video-processor (IC200) is used. The filtered IF signals are processed and sent as CVBS signal to the video switch IC (IC201). In IC201, according to the software and user control, the output CVBS signal is selected whether from the tuner, SCARTS, BAV, BAV or SVHS (or if exists DVD, DVB or else). The video IF signals from the SAW filters are processed in the video-processor, then sent as IF video output from pin 16. This output is again processed in the processor as CVBS signal from pin 24. The switched CVBS signal from IC201 is then processed as an input to pin 29. Then from pins 31/32/33 RGB signals are sent to the CRT baseboard as outputs. If there is an SVHS source the input signals from back or front SVHS jacks are input to pins 20/21 as chroma and luma respectively. If the TV is with comb-filter, both the CVBS and SVHS signals are filtered in the comb-filter IC (IC203). Then the outputs from IC203 are sent to video-processor.

SOUND PATH

The sound IF inputs (pins 8/9) are processed and sent as QSS output from pin 11 of IC200 to pin 58 of audio-processor IC700 as input. The sources other then IF are direct inputs to IC700. (SCARTS, FAV, BAV; pins 52/53/49/50/46/4743/44) These sound signals are processed and sent as outputs to audio amplifier IC701 (When Dolby Pro-logic or sub-woofer there are two audio-amplifiers.) or direct outputs from SCARTS, BAV, LINE OUT, HEADPHONE or else. If there are much more peripherals to give audio input, IC706 is used as a audio switch IC. In IC701, the main right and left audio signals are amplified and then given to the speakers. If the mute signal from the micro-controller comes, the amplifier is muted with hardware, the sound processor with software as well.

R.G.B

The R.G.B signals from pins 7,11 and 15 of the SCART connectors (PL207) are fed to the R.G.B input pins (41,42,43) of IC200.
R.G.B operation can be enabled by either taking pin 16 of the SCART connector high, this high is fed to Pin 44 of IC200 or via the I²C bus the micro-controller sets IC200 to forced R.G.B mode in which the video processor generates its own fast blank signal. This puts the IC into external R.G.B mode and selects the inputs on pins 41,42 and 43, overriding the video input on pin 24/29.
Note: when using R.G.B input the contrast, brightness and colour controls will still operate.

DEFLECTION CIRCUIT

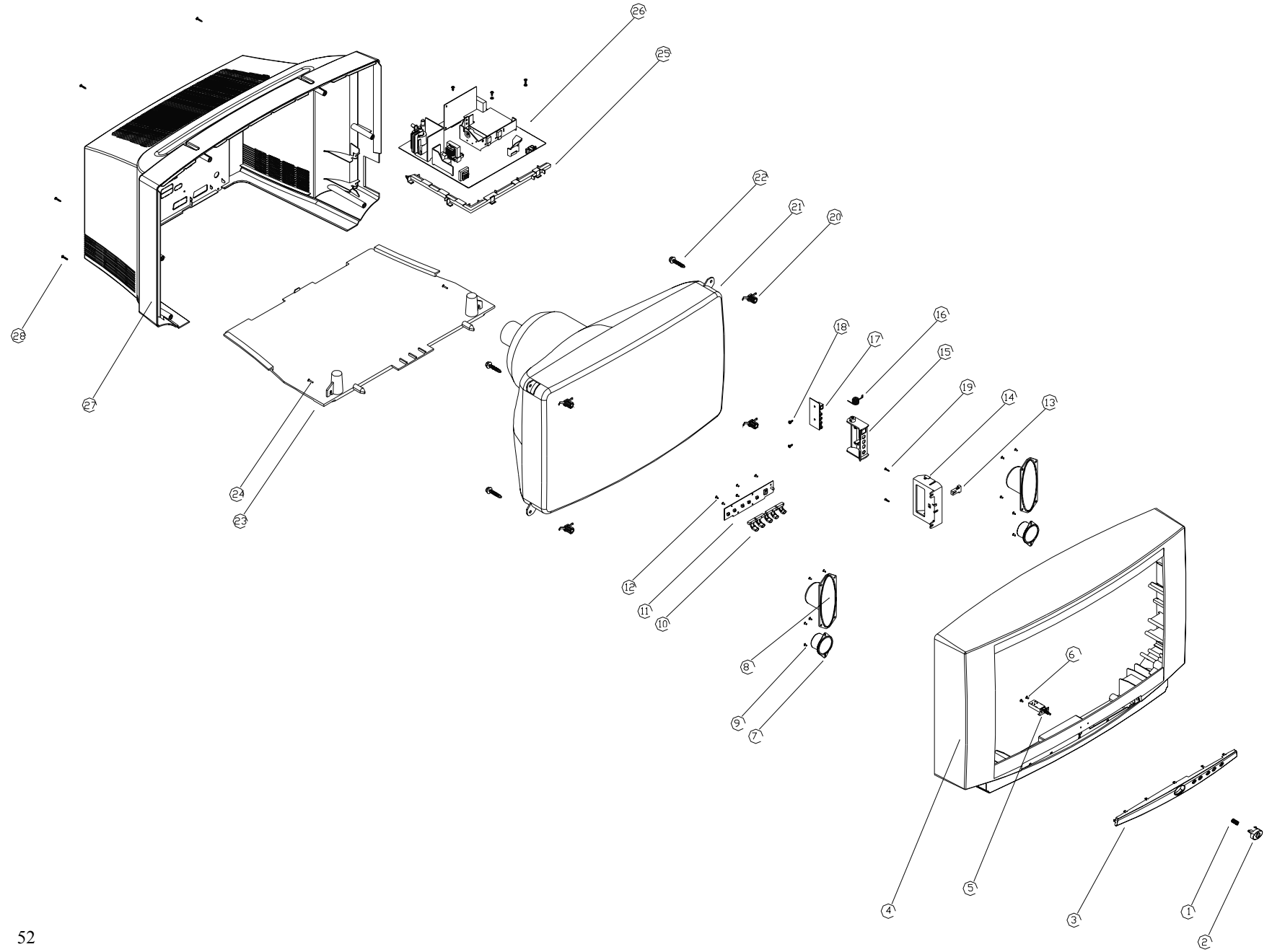
All the sync signals and drive signals for the deflection part are sent from the video-processor. A fly-back pulse is taken from pin1 of the FBT. The east-west (EW) signal from pin 62 of IC200 feeds the EW circuitry and Q604, so the horizontal deflection is enlarged and arranged according to the tube size. Sand (castle) signal from pin57 of IC200 is used for vertical and horizontal synchronisation. The horizontal level is driven by the horizontal-drive-out signal from pin 56 to Q600, through the TR600 horizontal transformer and finally the horizontal transistor Q602 is driven. FBT (TR601) is driven with the B+ supply voltage from the SMPS pin20. The vertical stage is processed by the vertical-deflection IC (IC600). The inverted and non-

inverted for this IC, is fed from pin63/64 of IC200. The outputs of IC600 are used for vertical deflection.

B.C.L CIRCUIT (BEAM CURRENT LIMITER)

Beam current limiting is employed to protect the circuitry in the receiver, the CRT and to prevent excessive X-ray radiation in fault conditions. The current drawn by the CRT is monitored by the current drawn through the winding of the fly-back transformer that produces the EHT for the CRT anode. The end of the winding (Pin 10) is returned to IC200 Pin 34, here according to the beam current info, low or high, brightness and contrast of the picture is set not to load the CRT with edge and maximum ratings. The beam current drawn by the CRT passes through Q602 and develops a voltage on the collector proportional to the current (V=IxR).

The voltage on the collector will vary depending on the beam current being drawn reducing the brightness and contrast of the picture. If the voltage is sufficiently negative (indicating very high excess beam current) the output will be reduced, reducing the picture brightness and contrast.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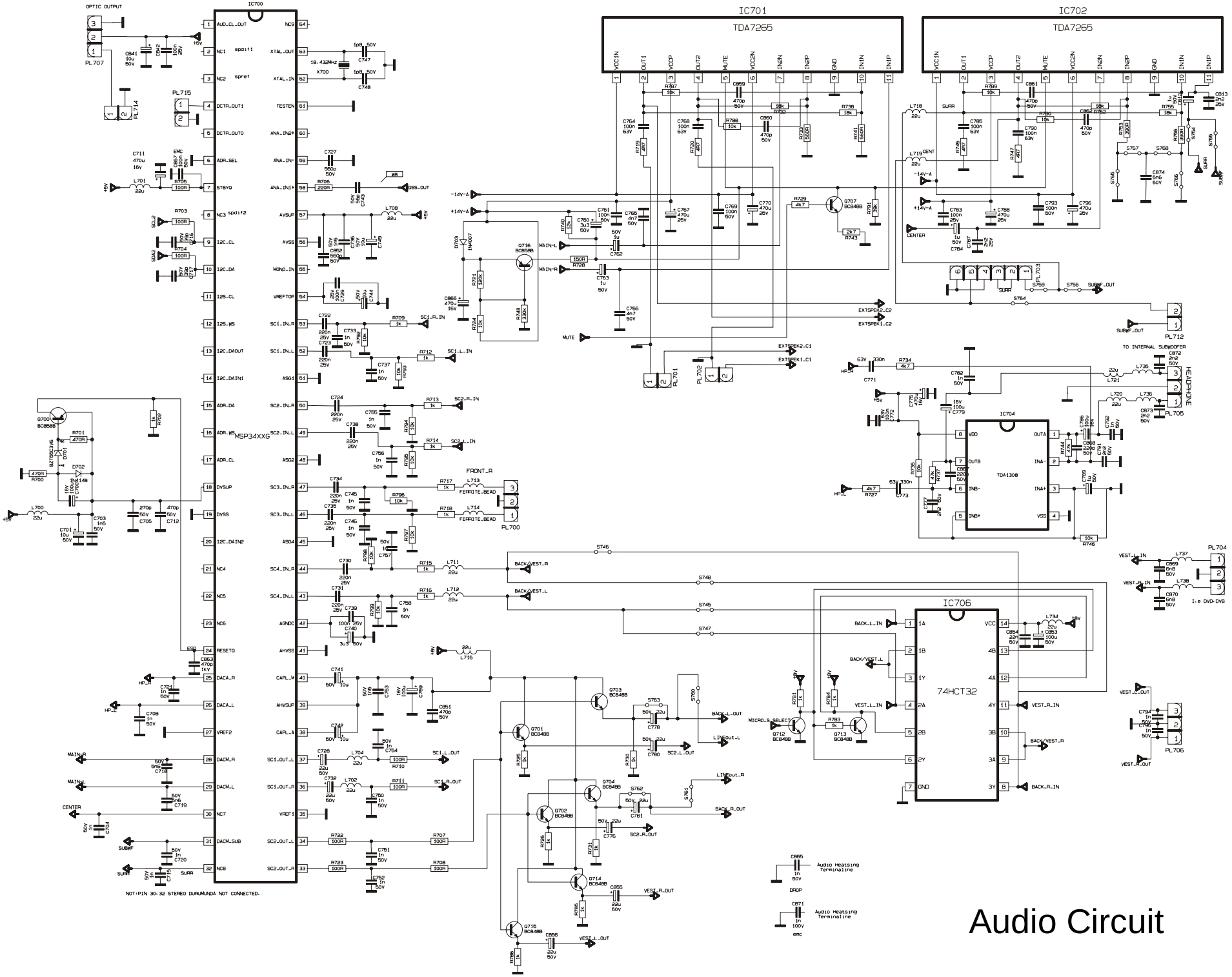
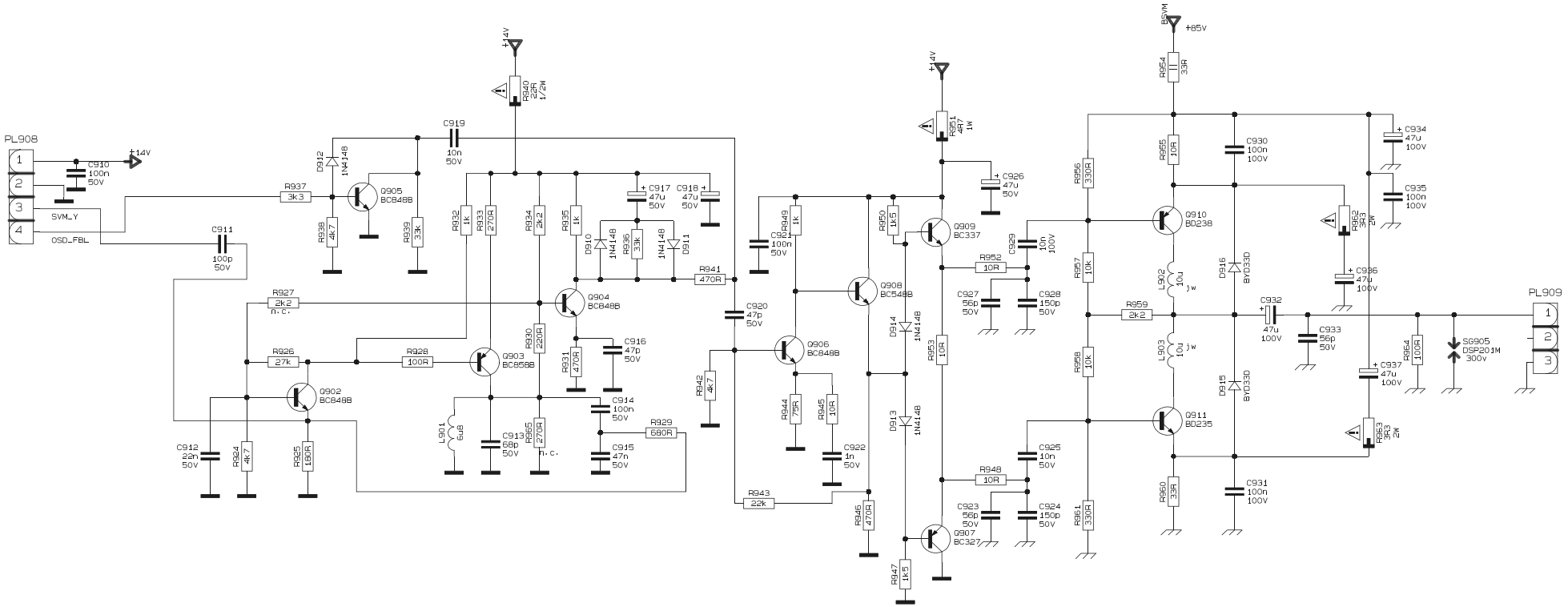
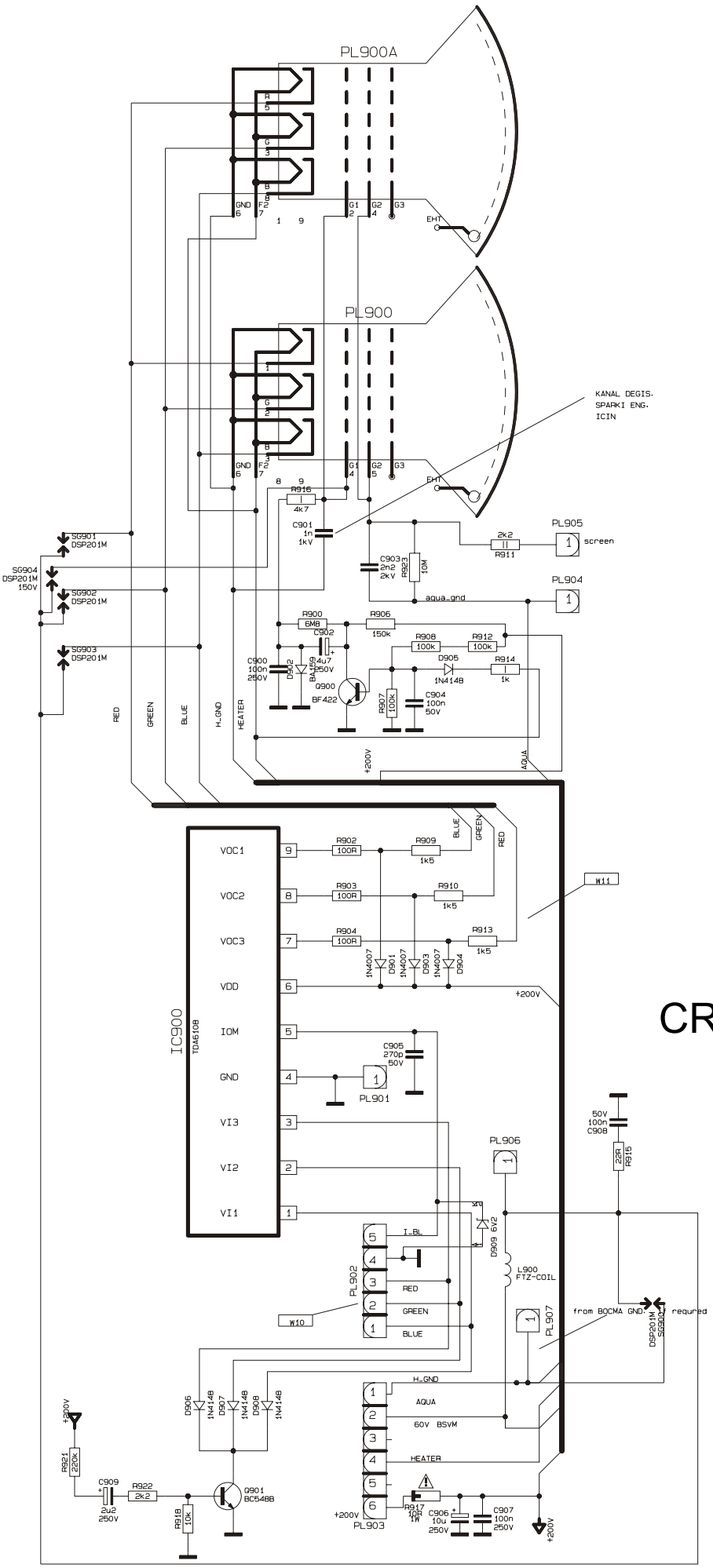
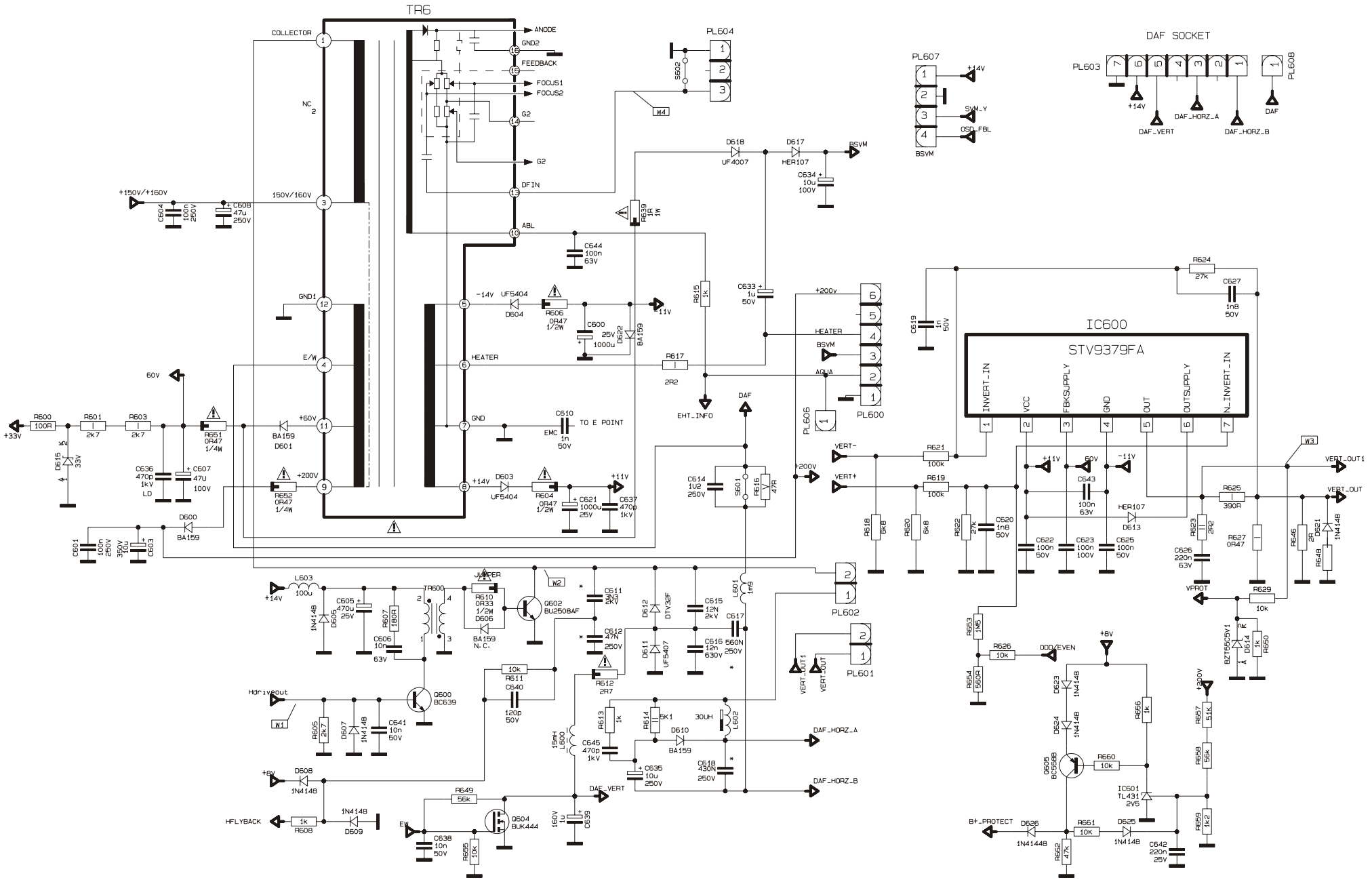

IC700
MSP34XXG
IC701
TDA7265
IC702
TDA7265
IC704
TDA1308
IC706
74HCT32
NOT-PIN 30-32 STEREO DURUMUNDA NOT CONNECTED.
Audio Circuit


PL908
SVM_Y
OSD_FBL
PL909
+14V
+85V
SVM
SG905
DSP201M
300V
Q902 BC848B
Q903 BC856B
Q904 BC848B
Q905 BC848B
Q906 BC848B
Q907 BC327
Q908 BC548B
Q909 BC337
Q910 BD238
Q911 BD235
D912 1N4148
D910 1N4148
D911 1N4148
D914 1N4148
D913 1N4148
D916 BYD33D
D915 BYD33D
L901 6u8
L902 10u
L903 10u
C910 100n 50V
C911 100p 50V
C912 22n 50V
C913 68p 50V
C914 100n 50V
C915 47n 50V
C916 47p 50V
C917 47u 50V
C918 47u 50V
C919 10n 50V
C920 47p 50V
C921 100n 50V
C922 1n 50V
C923 56p 50V
C924 150p 50V
C925 10n 50V
C926 47u 50V
C927 56p 50V
C928 150p 50V
C929 10n 100V
C930 100n 100V
C931 100n 100V
C932 47u 100V
C933 56p 50V
C934 47u 100V
C935 100n 100V
C936 47u 100V
C937 47u 100V
R924 4k7
R925 180R
R926 27k
R927 2k2 n.c.
R928 100R
R929 680R
R930 220R
R931 470R
R932 1k
R933 270R
R934 2k2
R935 1k
R936 33k
R937 3k3
R938 4k7
R939 33k
R940 22R 1/2W
R941 470R
R942 4k7
R943 22k
R944 75R
R945 10R
R946 470R
R947 1k5
R948 10R
R949 1k
R950 1k5
R951 4R7 1W
R952 10R
R953 10R
R954 33R
R955 10R
R956 330R
R957 10k
R958 10k
R959 2k2
R960 33R
R961 330R
R962 3R3 2W
R963 3R3 2W
R964 100R
n.c.

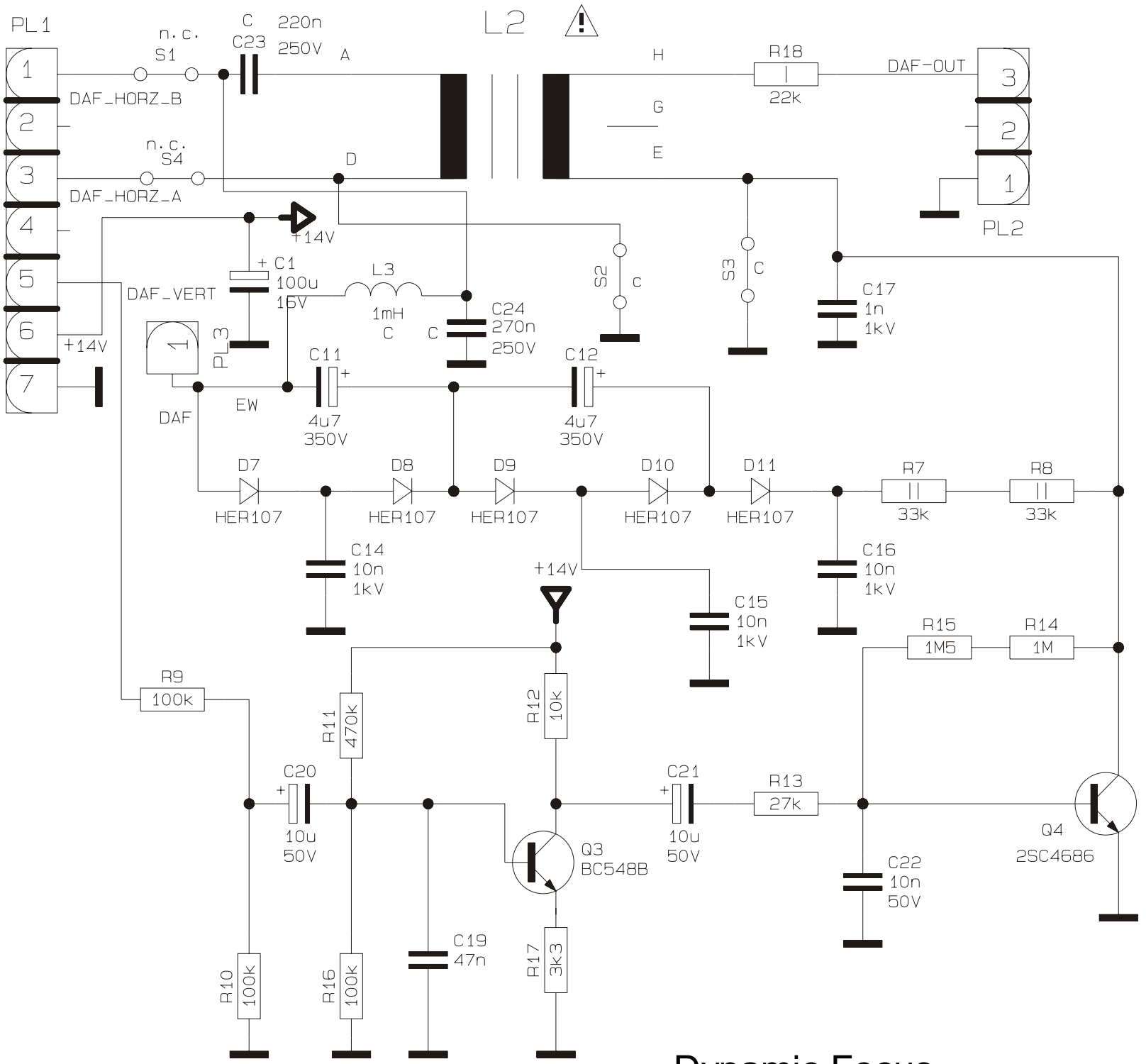
SVM Circuit


PL900A
PL900
KANAL DEGIS.
SPARKI ENG.
ICIN
EHT
R916
4k7
C901
1n
1kV
PL905
screen
2k2
R911
C903
2n2
2kV
R923
10M
PL904
aqua_gnd
S0901
DSP201M
S0904
DSP201M
150V
S0902
DSP201M
S0903
DSP201M
R900
6M8
R906
150k
C902
4u7
250V
R908
100k
R912
100k
C900
100n
250V
D902
BA159
D905
1N4148
R914
1k
Q900
BF422
R907
100k
C904
100n
50V
RED
GREEN
BLUE
H_GND
HEATER
+200V
AQUA
IC900
TDA6108
VOC1
VOC2
VOC3
VDD
IOM
GND
VI3
VI2
VI1
R902
100R
R903
100R
R904
100R
R909
1k5
R910
1k5
R913
1k5
1N4007
D901
D903
D904
W11
C905
270p
50V
PL901
PL906
50V
100n
C908
22R
R915
D909 6V2
L900
FTZ-COIL
PL902
I_BL
RED
GREEN
BLUE
W10
PL907
from BOCMA GND.
required
DSP201M
S0900
H_GND
AQUA
60V BSVM
HEATER
PL903
D906
D907
D908
1N4148
R921
220k
C909
2u2
250V
R922
2k2
R918
10k
Q901
BC548B
R917
10R
1W
C906
10u
250V
C907
100n
250V

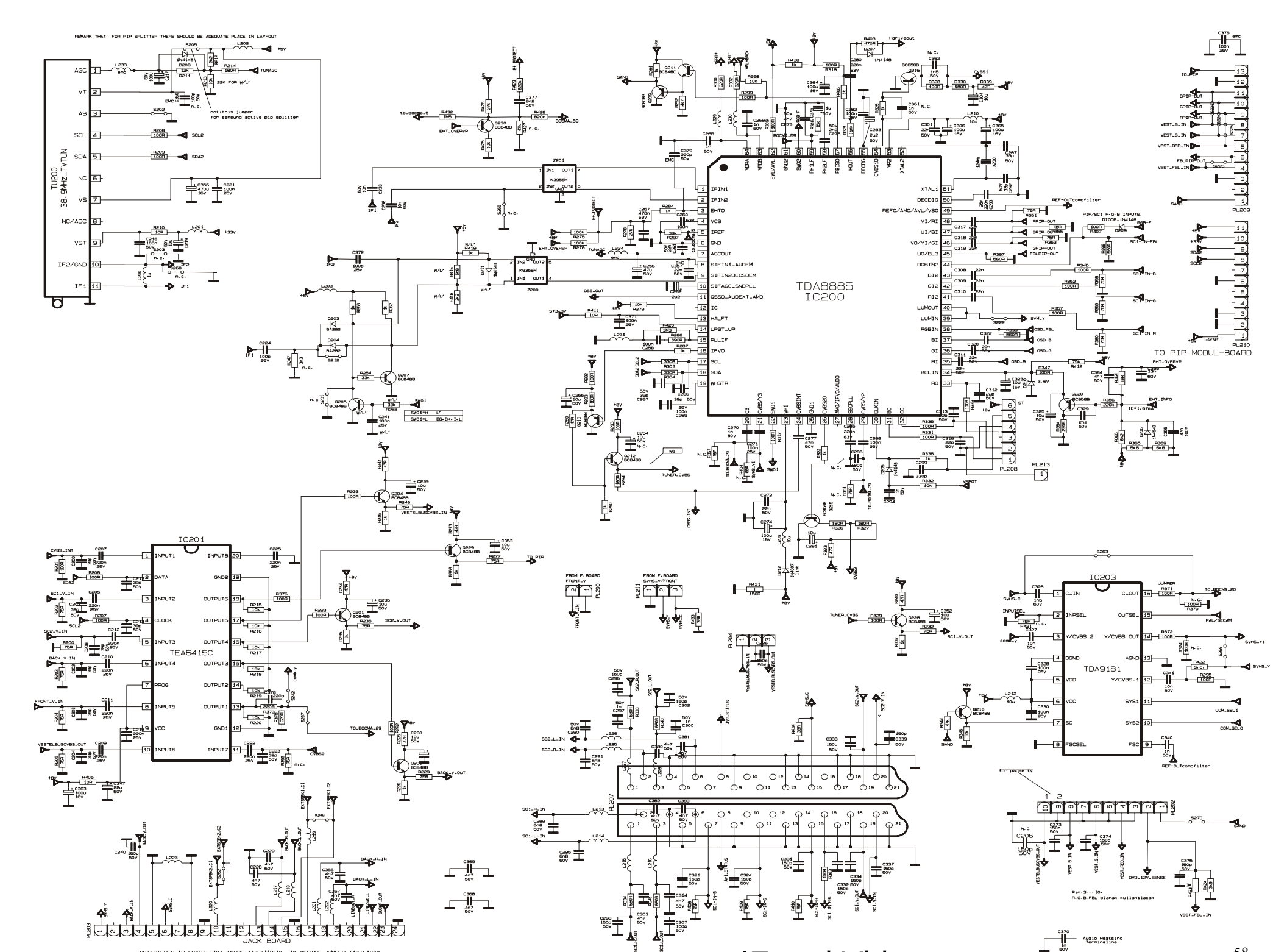
CRT



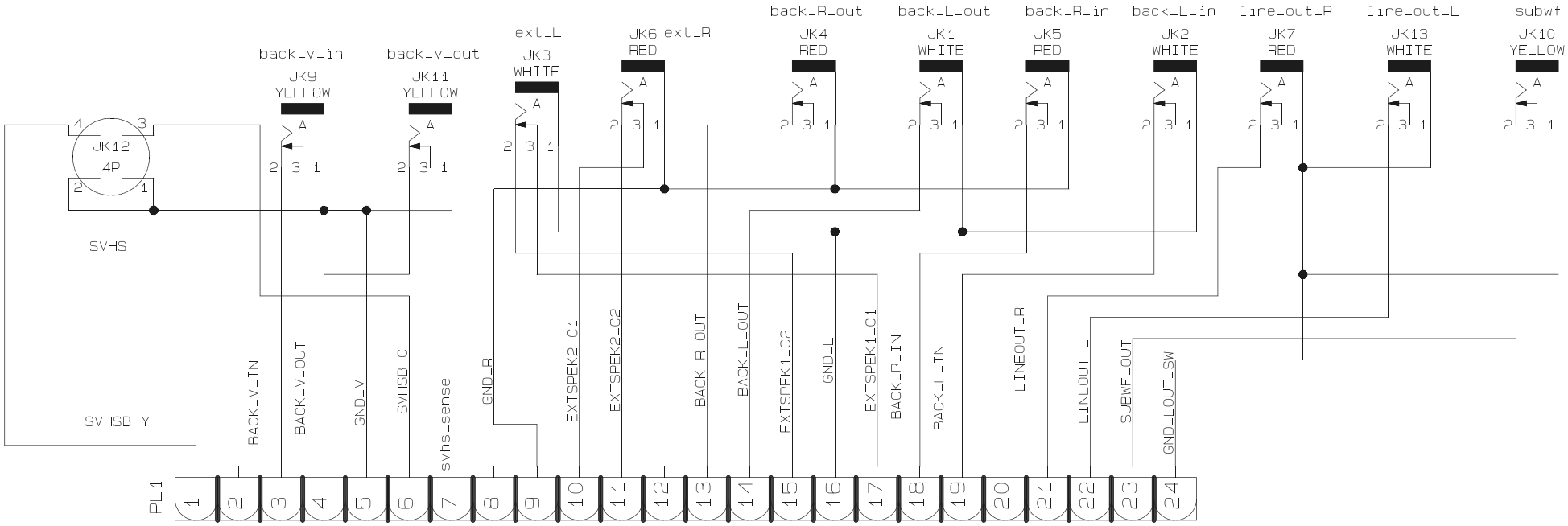
Deflection Circuit



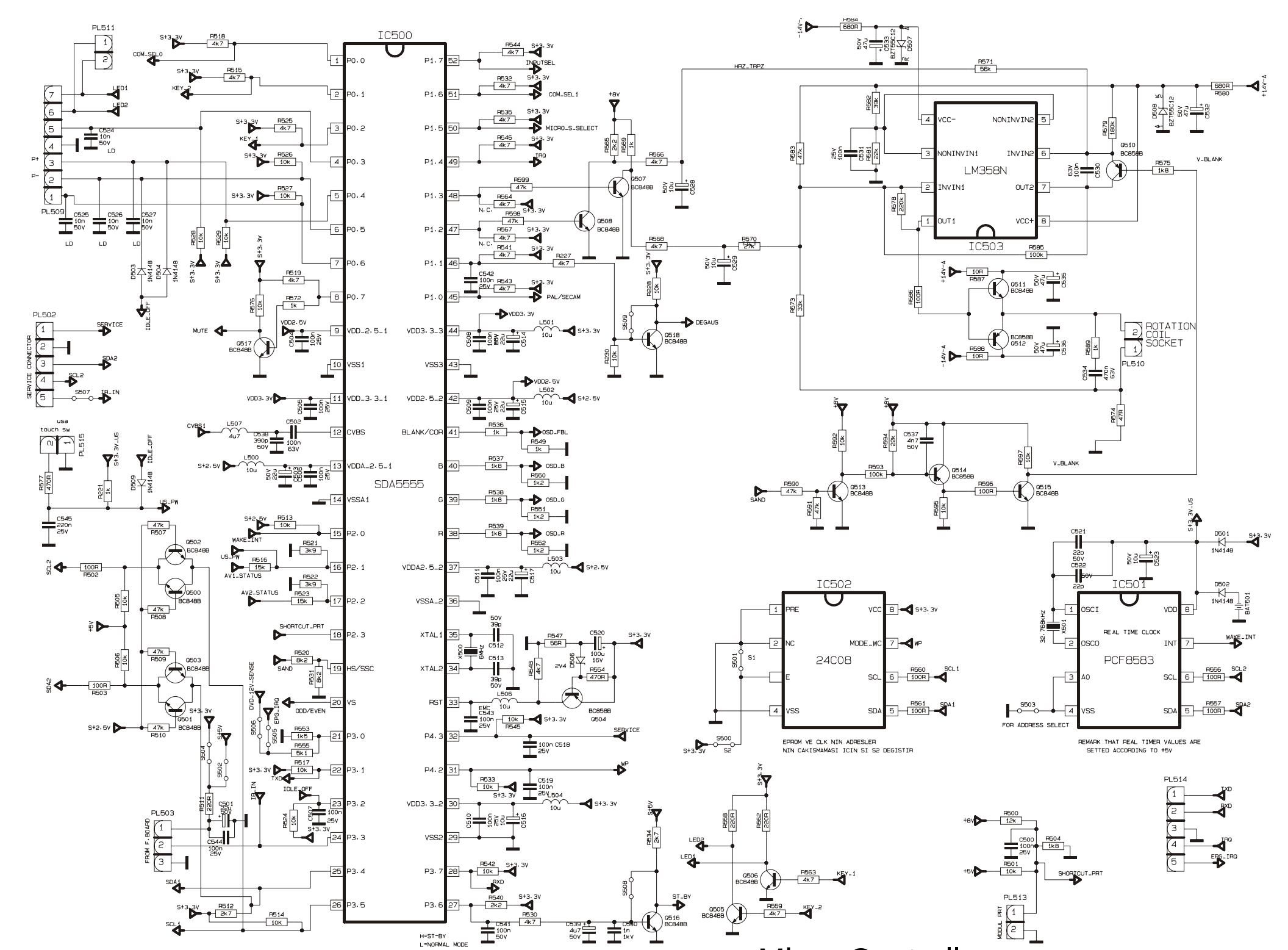
Dynamic Focus


TDA8885
IC200
TEA6415C
IC201
TDA9181
IC203
TU200
38.9MHz_TVTUN
JACK BOARD
TO PIP MODUL-BOARD
REMARK THAT. FOR PIP SPLITTER THERE SHOULD BE ADEQUATE PLACE IN LAY-OUT
NOT:STEREO AD SCART TAKI 150PF TAKILMICAK. 1K YERINE JUMPER TAKILACAK
DOLBY-AC-3 DE TAKILACAK.

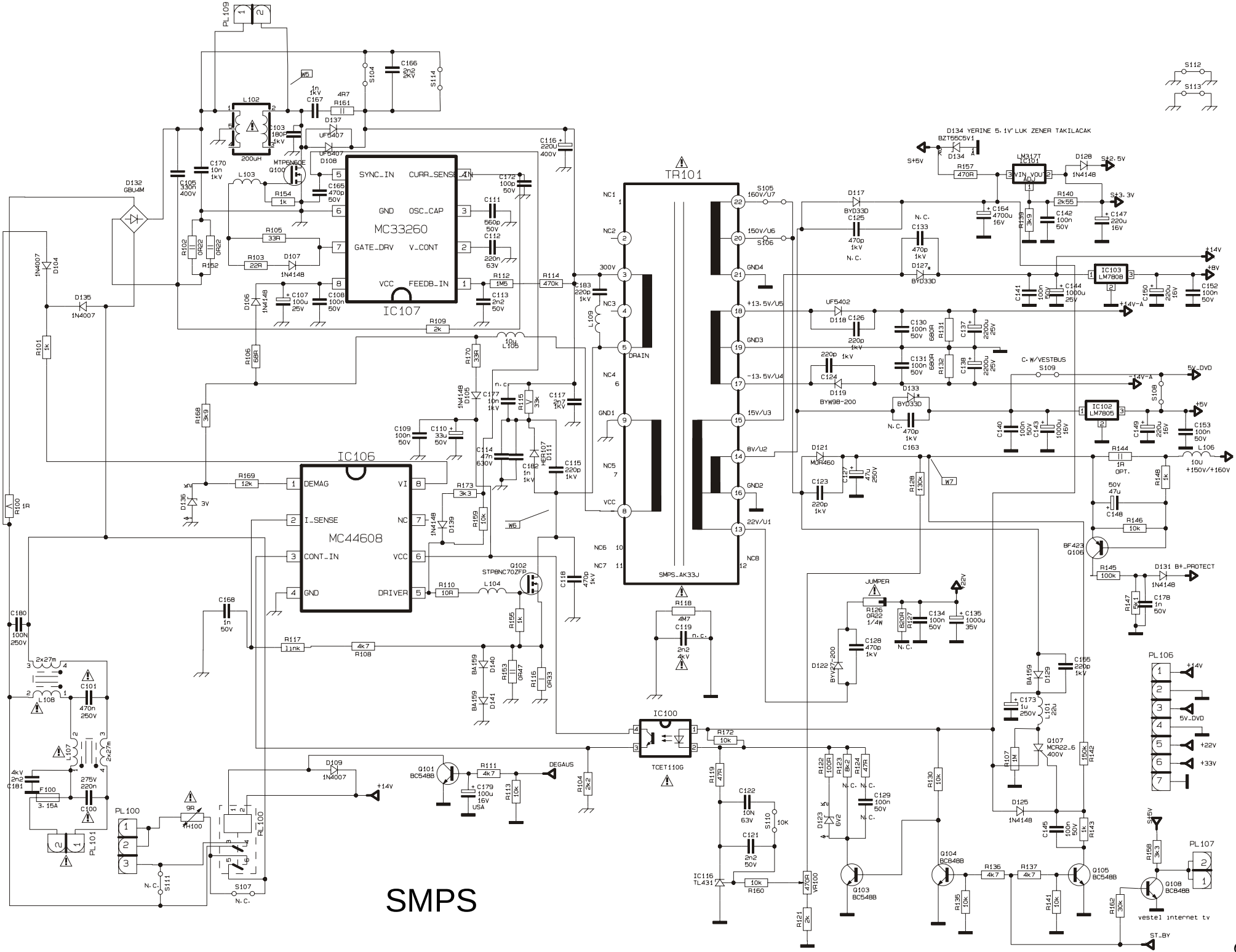
IF and Video


back_R_out
back_L_out
back_R_in
back_L_in
line_out_R
line_out_L
subwf
ext_L
JK6 ext_R
back_v_in
back_v_out
JK4 RED
JK1 WHITE
JK5 RED
JK2 WHITE
JK7 RED
JK13 WHITE
JK10 YELLOW
JK3 WHITE
JK9 YELLOW
JK11 YELLOW
JK12 4P
SVHS
SVHSB_Y
BACK_V_IN
BACK_V_OUT
GND_V
SVHSB_C
svhs_sense
GND_R
EXTSPEK2_C1
EXTSPEK2_C2
BACK_R_OUT
BACK_L_OUT
EXTSPEK1_C2
GND_L
EXTSPEK1_C1
BACK_R_IN
BACK_L_IN
LINEOUT_R
LINEOUT_L
SUBWF_OUT
GND_LOUT_SW
PL1

Jack



Micro-Controller


SMPS
MC33260
IC107
MC44608
IC106
TR101
SMPS_AK33J
TCET110G
IC100
IC116
TL431
IC103
LM7808
IC102
LM7805
IC101
LM317T
ADJ
D134 YERINE 5.1V' LUK ZENER TAKILACAK
BZT55C5V1
S+5V
S+2.5V
S+3.3V
+14V
+8V
+14V-A
5V_DVD
+5V
C.W/VESTBUS
S109
S108
B+_PROTECT
+150V/+160V
+22V
+33V
DEGAUS
ST_BY
vestel internet tv
PL100
PL101
PL106
PL107
PL109
RL100
TH100
S107
S111
S112
S113
S114
N.C.

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